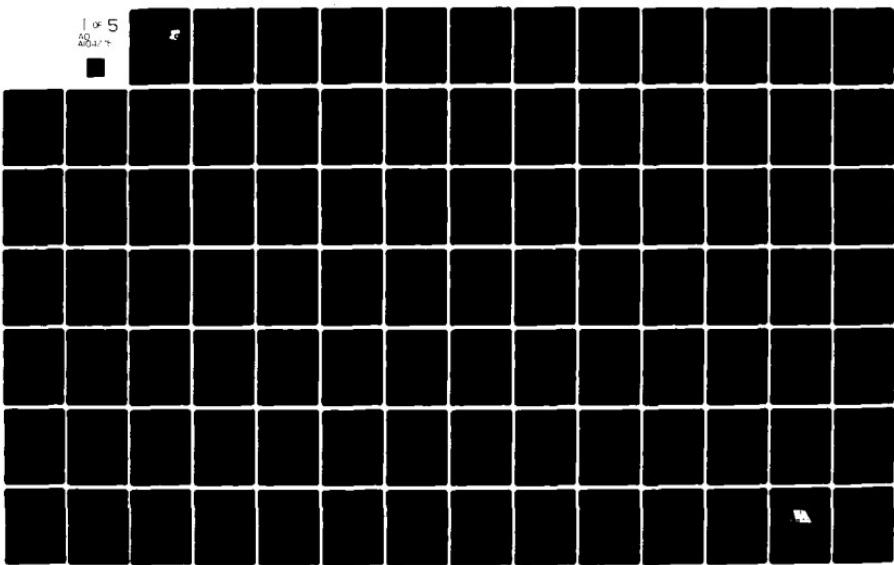


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APPLICATION OF PULSE CODE MODULATION (PCM) TECHNOLOGY TO AIRCRAFT DYNAMICS DATA ACQUISITION

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This technical report has been reviewed and is approved for publication.

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will result in a significant reduction in the cost of flight tests.

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FOREWORD

This report was prepared by the McDonnell Aircraft Company (MCAIR), St. Louis, Missouri for the Structural Vibration Branch, Structures and Dynamics Division, Flight Dynamics Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under Contract F33615-79-C-3205, "Application of Pulse Code Modulation (PCM) Technology to Aircraft Dynamics Data Acquisition". This contract was administered by Dansen Brown, Project Engineer, AFWAL/FIBG.

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SECTION I
INTRODUCTION AND SUMMARY

This report presents the results of a contracted design study for a flight test dynamic data system employing pulse code modulation (PCM). This study was performed by the McDonnell Aircraft Company (MCAIR), a component of the McDonnell Douglas Corporation. Assistance in the airborne system design was provided by MCAIR's subcontractor, SCI Systems, Incorporated. Assistance in the ground computer system studies was furnished by the McDonnell Automation Company (MCAUTO).

The study was performed in four phases as follows:

Phase I - Facility review, literature search, formulation of system standards and system goals (Appendix B).

Phase II - Definition of PCM systems (Appendices C and D).

Phase III - Evaluation of PCM systems (Appendix E).

Phase IV - PCM System Design (Sections I through VI, Appendix A, and References of this report).

As determined during the Phase I facility review, the Structural Vibration Branch of the Flight Dynamics Laboratory, Air Force Wright Aeronautical Laboratories (AFWAL/ FIBG) has a facility that provides dynamic data acquisition and analysis to support ground and flight testing on Air Force systems. This facility, based at Wright-Patterson Air Force Base (WPAFB), performs data acquisition at various geographical locations and subsequent data analysis back at the base. However, the current analog data acquisition system utilized for flight testing is limited to 12 channels of 40-50 dB dynamic range. Also, the current analysis system at the facility is difficult to program, has severely limited memory capacity, and suffers from the inaccuracies of fixed-point (rather than floating-point) processing. By contrast, in order to solve vibration and noise-related problems in complex aircraft structures, 100 or more simultaneously acquired accurate measurements from different locations are frequently required. Analytical tools have been available for some time to solve complex structural problems if such measurements were available, along with a computer facility of sufficient

capability to handle the data. Continued use of existing facilities will result in less than optimal usage of people and other resources such as aviation fuel, as well as unnecessary delays in obtaining solutions to structural problems.

The PCM system design presented herein is optimized for the goals and requirements of AFWAL/FIBG. It includes an airborne PCM acquisition and recording system, and a ground system for playback, editing, and analysis. Key features are the ability of the airborne system to acquire and record data from up to 144 20-KHz analog transducers simultaneously for up to eight hours, and sufficient computer power and memory capacity in the ground system to process the large amount of resulting data (approaching a maximum of 10^{11} bits recorded per flight). Onboard tape recording is the only practical means of storing such large quantities of data acquired in flight tests at various remote sites for later processing at AFWAL/FIBG's home base.

The airborne PCM encoder/formatter system and its associated ground support equipment will require approximately two years of detailed design and development activity in order to be realized. The maximum data rate capacity of this system will be approximately 154 megabits per second (48 serial streams of 3.2 megabits per second each). This exceeds that of existing aircraft flight test PCM systems by two orders of magnitude.

The ability of existing tape recorders and tapes to absorb data at the above rate and reproduce with a satisfactory bit error rate (BER) performance can best be determined by experiment. Therefore, prior to initiating development of the airborne system, MCAIR recommends that a tape recorder/reproducer evaluation be performed. A PCM simulator and a BER tester will be needed for this evaluation.

The ground support equipment to be developed consists of a format memory programmer (for setup of the airborne system), an integrated test set (used for checkout and maintenance of the system), and a quick-look test set.

Other hardware items that are not off-the-shelf (and, therefore,

requiring development) include a multiple decommutator multiplexer and computer interface and a high-speed bus-converter interface between the computer and array processor.

The recommended ground processing system consists of a Digital Equipment Corporation VAX 11/780 host computer and a Floating Point Systems, Incorporated AP180V array processor, and associated peripheral equipment. This system would replace AFWAL/FIBG's current Raytheon 704 facility, which is insufficient to manage the increased amount of source data acquired by the new airborne system.

In addition to the hardware, considerable new software development is required to support new features of the ground processing system. Some software development will also be needed for the format memory programmer and integrated test set.

Although the data system developed during this study meets the primary design performance goals, it exceeds the targeted values for the airborne system power, weight and size. Recommendations are provided for further study in this area and related hardware evaluation. A milestone development schedule is provided.

SECTION II

FLIGHT TEST DYNAMIC DATA ACQUISITION - STATE-OF-THE-ART

Flight test data can be categorized according to how rapidly it is expected to change. Some data (for example, takeoff empty weight) are, by definition, constants for a given flight. These are called "static" measurands because they are completely described by a single measurement. Other measurands, such as structural temperatures, are expected to change during flight, although for a given set of flight conditions they may be constant. These measurands, which may be characterized by relatively infrequent measurements, are called "quasi-static". Acoustic noise, vibration and strain are examples of dynamic data. Signals from dynamic transducers oscillate rapidly (usually in random fashion) and require either continuous monitoring or high-speed sampling in order to recover the desired information. The information contained in these signals is then condensed for the analysts' interpretation by computing various statistical and/or spectral properties.

Currently, aircraft dynamic data is generally recorded or telemetered in analog form, using either amplitude modulation (AM) or frequency modulation (FM) techniques. Where tape recording of analog dynamic signals is required, FM is used so that signal distortion by the frequency response characteristics of the recorder/reproducer is minimized [1]. In order to transmit multiple analog measurands over a single communication channel (i.e., tape track or RF telemetry link), frequency division multiplexing is often employed. However, the current AFWAL/FIBG system uses a separate tape track for each measurand, employing single-carrier FM.

Until 1965, analog recordings of dynamic data were necessary because analysis methods available prior to this were primarily analog (see Figure 1). Since 1965, efficient digital signal processing algorithms and faster and cheaper digital computer hardware have evolved together so as to render analog signal analysis virtually obsolete. AFWAL/FIBG has exploited the advantages of digital processing techniques with its Raytheon 704 computer and array transform processor. The recorded analog data is played back and

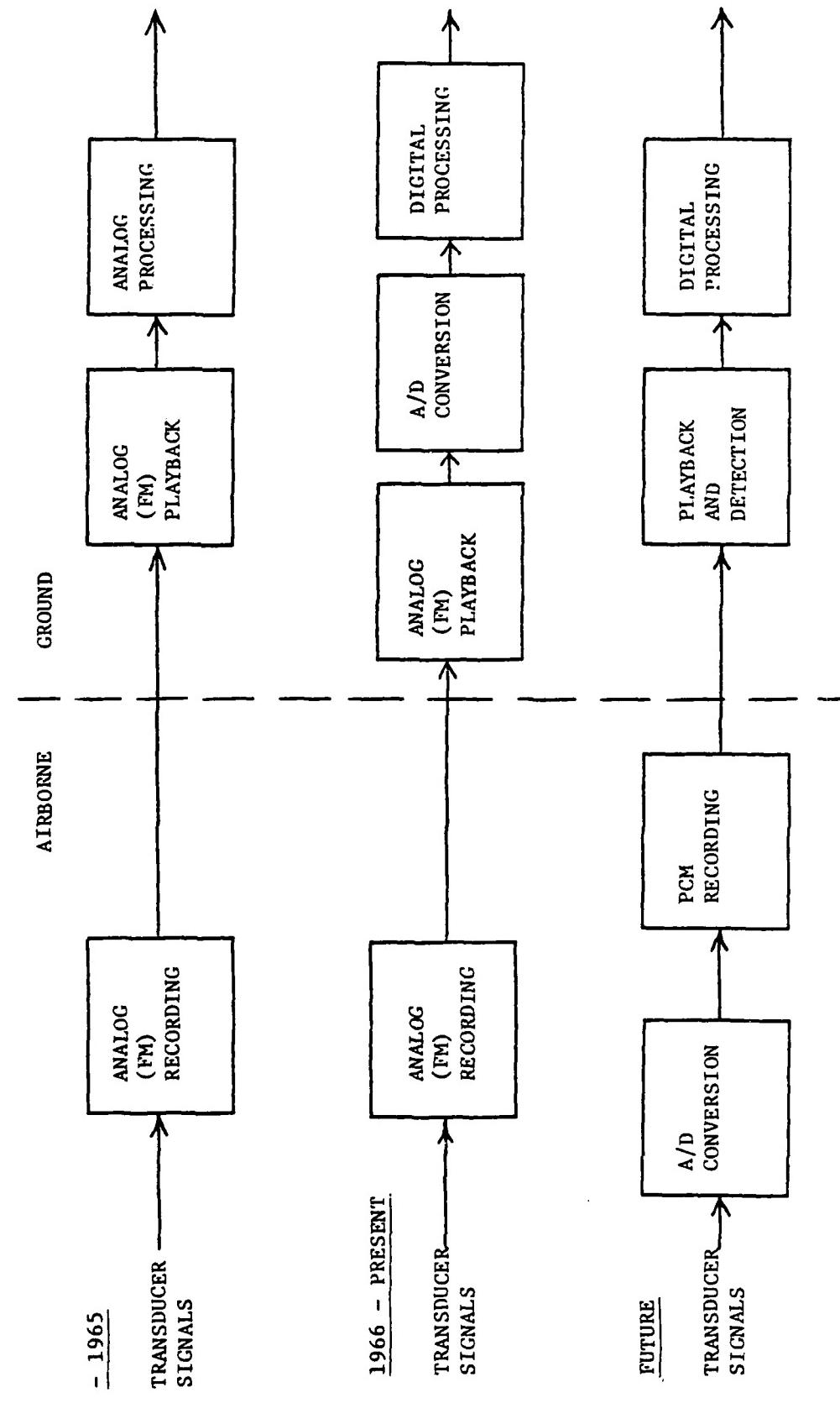


FIGURE 1
HISTORICAL DEVELOPMENT - RECORDING AND PROCESSING OF AIRCRAFT DYNAMIC DATA

segments of interest are sampled and converted to digital words (using an analog-to-digital converter) for entry into the computer for processing. Thus, the data is still recorded via FM even though all digital processing is used.

The current AFWAL/FIBG FM system provides adequate bandwidth (20 KHZ) for each measurand channel; however, only 12 such channels are available. AFWAL/FIBG test requirements often dictate that data be acquired simultaneously from 100 or more measurands so that correlation and coherence among the various transducer responses can be studied. Thus, non-concurrent measurand acquisition achieved by switching the instrumentation to a new set of measurands and repeating test conditions is not a solution. Another major deficiency of the present system is that its signal-to-noise ratio (dynamic range) is limited to 50 dB at best, while analysts have long desired 60-70 dB [2]. This limitation is caused primarily by speed variations (flutter) in the tape recorder. Frequency division multiplexing could be employed to increase the number of data channels; however, this would result in a compromise in measurand bandwidth and would degrade rather than improve the dynamic range.

Pulse code modulation is a form of time division multiplexing featuring analog to digital conversion. With its multiplexing capability, multiple measurands per tape track can be employed, and the incorporation of the analog-to-digital conversion prior to recording increases the dynamic range.

SECTION III
PCM TECHNOLOGY - STATE-OF-THE-ART

Using PCM, data is encoded in digital form prior to recording. Thus, the effects of noise and distortion (including inter-track time delays) in the record/reproduce process no longer affect the dynamic range or inter-channel phase characteristics of the data. Thus dynamic range and inter-channel phase accuracy are limited only by transducers and the electronics used for signal conditioning transducers and the encoding. The digital data, when recovered from the tape, can be inputted to a computer for editing and further processing. Also, the use of PCM recording makes it easy to employ applicable data compression techniques in order to conserve recorder bandwidth, thereby, extending the record time capability.

PCM has been used in flight testing for approximately 20 years [3]. However, except in rare instances, its application has been confined to low frequency or quasi-static data, for which time history records are desired [2]. At AFWAL/FIBG, high-frequency dynamic data are still being recorded with FM (even though digital processing has replaced analog analysis methods, and hence, there is no longer any real need to retain the continuous analog signals). This is due primarily to the data rate limitations of available PCM encoding equipment.

Table 1 shows a comparison of characteristics of the PCM system recommended for AFWAL/FIBG with those of three aircraft flight test PCM systems currently in use. A key feature of the recommended system is that it will have sufficient bit rate capacity to simultaneously achieve the maximum number of measurands and the maximum sample rate per measurand. This is in contrast to the existing PCM systems which have limited bit rate capacity so that the number of measurands and sample rate for each must be traded off.

One way to increase the number of available measurand channels with a limited bit rate capacity is to reduce the data rate required for each measurand by data compression. However, the usual compression techniques used in connection with quasi-static data

TABLE 1
COMPARISON OF AIRBORNE PCM ENCODER/FORMATTER CHARACTERISTICS

SYSTEM	TDMS	ATIS	PDAS	RECOMMENDED
MANUFACTURER	SCI	SCI	BASE TEN	
USER	MCAIR	AFFIC	ADTC	AFVAL/FIRG
TOTAL BIT RATE	0.0288 MB/SEC	0.512 MB/SEC	1.2 MB/SEC	154 MB/SEC
MAXIMUM NUMBER OF ANALOG MEASURAND CHANNELS	480	960	1536	144
MAXIMUM SAMPLE RATE	720 S/SEC	21,333 S/SEC	50,000 S/SEC	65,536 S/SEC
DATA RESOLUTION	8 BITS	10 BITS	11 BITS	12 BITS
RANGE SETUP				
A) GAIN	FIXED	FIXED	FIXED	AUTOMATIC
B) OFFSET	FIXED	FIXED	FIXED	NONE
MAXIMUM NUMBER OF TAPE OUTPUTS	1	4	1	48

are not applicable to dynamic data. There are no redundant sample points to discard; the degree of correlation between adjacent sample values is one of the things to be ascertained in the analysis - not discarded beforehand! There are, however, onboard analysis techniques applicable to dynamic data that can reduce the data rate by one to three orders of magnitude. A summary of the available techniques is included in Appendix B. Onboard analysis such as 1/3 octave processing is useful in some applications; however, it does limit the options available to the analyst once the data has been acquired. In particular, it is not satisfactory where large numbers of cross-channel analyses must be performed. Appendix B also describes a data compression method for dynamic signals which does not involve any form of analysis. This is the multiple filter encoding method which has been incorporated as a design feature of the recommended PCM system. This method provides sequential bursts of data sampled from a series of lowpass filters of different bandwidths rather than data continuously sampled from the overall bandwidth of interest. Application of this method is limited to test conditions such that the data is stationary for at least 11 seconds with minimal frequency resolution requirements or 3 minutes with maximum resolution.

Thus, the data compression represents only a partial solution to the problem of accommodating a large number of dynamic measurand channels in a PCM system. Clearly, higher data rates are needed than are presently available in flight test PCM hardware. The maximum bit rate for AFWAL/FIBG requirements and goals has been calculated in Appendix C to be 154 megabits per second. This is based upon 144, 20-KHz measurand channels with no data compression.

However, the maximum bit rate that can be recorded is a function of the bandwidth available in the tape recorder/reproducer system. Considering the non-return to zero (NRZ) PCM codes, which are the simplest and require the least bandwidth, the highest bit rate that can be recorded is equal to twice the direct record bandwidth. Thus, at least 77 MHz total recorder bandwidth is required for AFWAL/FIBG's maximum bit rate.

Figure 2 shows the historical progress of bandwidth capability of recorder/reproducers per IRIG standards [4], [5], [6], [7]. It should be noted that airborne recorder capabilities have lagged the IRIG standards. The Sangamo Sabre XII recorder meets the 1977 standards (28 tracks with a 2-MHz response at 120 inches per second) with an overall bandwidth of 56 MHz. Thus, more than one such recorder will be required in order to handle AFWAL/FIBG's maximum data rate.

For a 144-measurand channel system, 48 tape tracks of two 28 track recorders can be employed to record 3 measurands each in serial PCM streams. The 48 tape tracks represents 96 MHz of total direct record bandwidth. Since 77 MHz has been established above as the minimum bandwidth necessary, this solution is potentially a satisfactory one.

However, this ignores signal-to-noise and bit-error-rate considerations in the recorder/reproducer and the PCM detection device (bit synchronizer). All tape recorder devices have poor low-frequency response (zero response at DC), yet NRZ PCM can have considerable low-frequency content, depending on the data activity. This results in potentially unsatisfactory performance (loss of synchronization and data dropouts). Therefore, for tape recording, the NRZ must be modified in some manner to reduce its low-frequency content. All such modifications result in an increase in required bandwidth for a given bit rate, or equivalently, an increase in required signal-to-noise ratio to maintain a given level of bit-error-rate performance. The effects of recorder/reproducer noise and distortion on the digital data will result in an occasional error in reading the encoded sample values. The theoretical bit-error probability (BEP) versus signal-to-noise ratio can be calculated as follows [8]:

$$BEP = \sqrt{\frac{1}{2\pi}} \int_x^{\infty} \exp\left[\frac{-\alpha^2}{2}\right] d\alpha \quad (1)$$

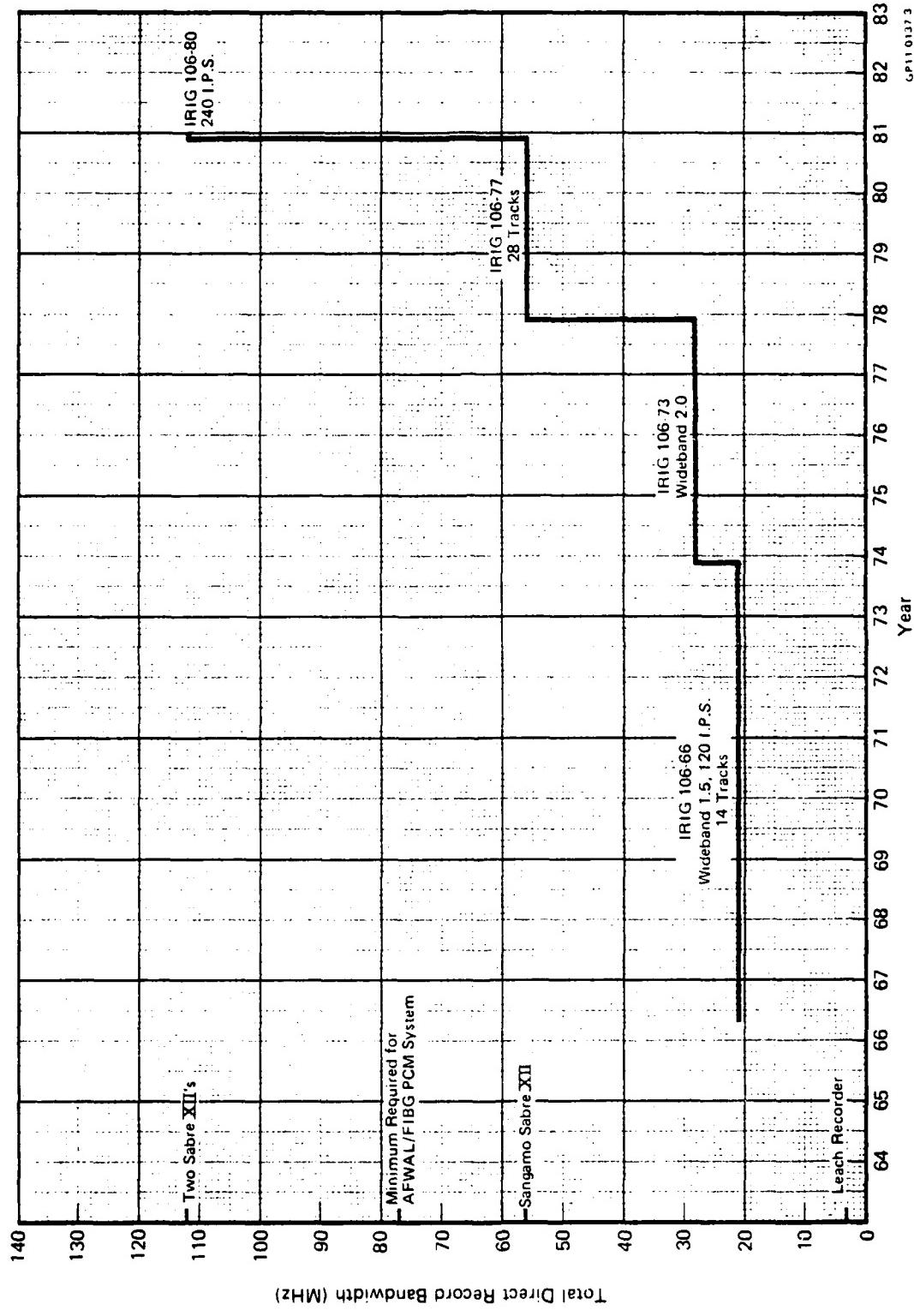


FIGURE 2
TAPE RECORDER TECHNOLOGY
BANDWIDTH OF IRIG WIDEBAND RECORDERS

where: $x = 10^{\frac{dB}{20}}$

dB = 1/2 peak-to-peak signal to RMS noise ratio in dB

BEP = bit error probability (multiply by bit rate to get bit error rate)

The NRZ code modification adopted in IRIG 106-80 for serial high density PCM tape recording is RNRZ-L (Randomized NR -Level). This modification results in the least performance decrease of all the known serial encoding methods. It does triple the bit error rate, which is equivalent to an increase of .43 dB (in the vicinity of 10^{-6} BEP) in signal-to-noise ratio required to maintain a given BEP. The .43 dB can, in turn, be regained by reducing the recorded bit rate and, hence, the bit packing density [9]. IRIG recommends a maximum density of 25,000 bits per inch per track. The MCAIR recommended tape recorder configuration results in a tape packing density of 26,800 bits per inch, thus exceeding the IRIG limit. However, manufacturers of recorders and PCM bit synchronizers claim [10], [11] satisfactory performance using RNRZ-L at 30,000 bits per inch.

Whether or not the recommended configuration will result in a satisfactory bit-error-rate performance with the recorder in an airborne environment should be determined experimentally. If operation at 26.8 kilobits per inch proves unsatisfactory, 144, 20-KHz channels could be accommodated with three 28-track 120-ips recorders using 72 tracks at 17.9 kilobits per inch.

The advantages of PCM for AFWAL/FIBG's dynamic data application are as follows:

- ° Dynamic range of 66 dB - made possible by digital encoding prior to recording.
- ° 144 simultaneously acquired measurands - by using simultaneous encoding and wide-bandwidth 28-track recorders.
- ° Up to 8 hours record time for 20-KHz data - made possible by data compression.
- ° Easy data entry into ground system computer - by use of 16-bit digital data format.

A disadvantage of PCM is that the data must be bandwidth-limited to the analysis range prior to acquisition.

SECTION IV

SUMMARY OF STUDY PHASES I, II, AND III

1. COST DISCLAIMER

The remainder of this report contains cost information for various systems and components. In all cases, this information should be considered as approximate; it is furnished as engineering evaluation reference for budgetary and planning purposes only. All prices mentioned are in terms of 1980 dollars; no attempt has been made to adjust for inflation trends or potential discounts. Sources for the cost information (in addition to the latest published catalog information) include:

- SCI Systems, Incorporated (non-recurring and recurring estimate for airborne encoder/formatter system);
- DSI Cost Quotation No. 100-142-026 (decommutation, multiplexer and computer interface);
- Sangamo Negotiation No. 99036101 (airborne tape recorders).

This report should not be construed as an offer by MCAIR or its subcontractor, SCI Systems, Incorporated, or other suppliers to supply the equipment or services described herein.

2. LITERATURE SEARCH

The primary focus of the Phase I literature search was on-board compression techniques for dynamic data acquisition. The result was that, given AFWAL/FIBG analysis requirements, multiple filter encoding can be employed to extend the available record time for stationary data; however, for non-stationary or transient data, continuous sampling is required. AFWAL/FIBG's requirement for multi-channel analyses (e.g., correlation, coherence, and transfer functions) was a crucial factor in this conclusion, since the literature search uncovered some onboard digital data compression techniques, such as bandpass filter analysis, that are suitable for single-channel analysis. Further details of the literature search, including abstracts of pertinent literature, are found in the Phase I Interim Report (Appendix B).

3. GOALS AND REQUIREMENTS VERSUS PROJECTED PERFORMANCE OF RECOMMENDED SYSTEM

Tables 2, 3, and 4 summarize the projected performance of the recommended system. This data is compared to design goals and requirements established in this study in terms of standards for comparison which were also developed in the study. Details pertinent to the projected performance are found in Appendix A. An evaluation of the AFWAL/FIBG data system (as it existed on 1 June 1979) and development of the standards and goals are documented in Appendix B (Phase I Interim Report).

As indicated in Table 2, the recommended airborne system falls short of the goals established for volume, weight, and power. The following table provides a comparison of the total airborne volume, weight and power with the existing FM system on a per channel basis.

AFWAL/FIBG WBFM SYSTEM	GOAL	PROJECTED PERFORMANCE PCM SYSTEM
VOLUME (CU IN/CH)	570.00	24.00
WEIGHT (LB/CH)	9.17	0.35
POWER (WATTS/CH)	9.33	0.78

Currently available airborne tape recorders do not meet MIL-E-5400 Class 2 low temperature requirements. The two Sangamo Sabre XII recorders assumed for study purposes are specified to operate down to -20°C, and can go as low as -40°C with optional heater elements. Power for the heaters is unspecified; therefore, it is not included in the total of 1372 watts shown in Table 2. Reliability of the Sabre XII recorder is also unspecified; therefore, it is not included in the 898 hour MTBF figure.

4. DESIGN APPROACHES

The following study areas were analyzed in order to formulate system candidates for evaluation.

- (1) Alternate configurations and flexibility of multiple filter encoding.

TABLE 2
ACQUISITION PROCESS
GOALS AND REQUIREMENTS VERSUS PROJECTED PERFORMANCE
OF RECOMMENDED PCM ENCODER/FORMATTER AND AIRBORNE RECORDERS

STANDARD	GCAL. * REQUIREMENT	PROJECTED PERFORMANCE
1. BANDWIDTH/MEASURAND	DC TO 20 KHZ (+1 DB) *	DC TO 20 KHZ (+1 DB)
2. ACCURACY	.5% @ DC	.83%
3. ENCODING RESOLUTION	12 BITS PLUS 3 BITS AUTO-RANGE	12 BITS PLUS 3 BITS AUTO-RANGE
4. DYNAMIC RANGE	66 DB PLUS 70 DB AUTO-RANGE	66 DB PLUS 70 DB AUTO-RANGE
5. NUMBER OF MEASURANDS	144 *	144
6. INTER-CHANNEL PHASE ERROR	5° @ 10 KHZ	3°
7. RECORD TIME	A) TRANSIENT B) STATIONARY	7.5 MINUTES 8.0 HOURS
8. PHYSICAL	A) SIZE B) WEIGHT C) MODULARITY	2.0 CUBIC FEET 50 POUNDS N.D.
9. ENVIRONMENTAL CONDITIONS	MIL-E-5400, CLASS 2	MIL-E-5400, CLASS 2 \triangle_1
10. POWER	112 WATTS @ 28 VDC	1372 W.
11. RELIABILITY	1000 HOURS	898 HOURS \triangle_1
12. MAINTAINABILITY	N.D.	-
13. TEST READINESS	N.D.	-
14. CAPABILITY FOR ON-SITE EVAL.	ALWAYS	ALWAYS
15. OPERATIONAL FLEXIBILITY	N.D.	-
16. RECURRING PERSONNEL SUPPORT	N.D.	-
17. SYSTEM HARDWARE COSTS	N.D.	\$868,000 (NR); \$439,930 (R) \triangle_2

N.D. = GOAL NOT DECLARED.

\triangle_1 = EXCLUDING TAPE RECORDERS.

\triangle_2 = EXCLUDING ACR AMPLIFIERS.

NOTE: REFER TO APPENDIX A FOR DETAILS OF PROJECTED PERFORMANCE.

TABLE 3
 ANALYSIS PROCESS
 GOALS AND REQUIREMENTS VERSUS PROJECTED PERFORMANCE
 OF RECOMMENDED GROUND PROCESSING SYSTEM

STANDARD	GOAL	PROJECTED PERFORMANCE
MAXIMUM ARRAY SIZE	16,384 16 BIT WORDS	32,768 38 BIT WORDS
CHOICE OF ANALYSIS TYPES		
AUTO PSD	YES	YES
CROSS PSD	YES	YES
AMPLITUDE SPECTRA	YES	YES
TRANSFER FUNCTION	YES	YES
COHERENCE	YES	YES
MODAL ANALYSIS	YES	YES
ZOOM TRANSFORM	YES	YES
1/3 OCTAVE ANALYSIS	YES	YES
RMS TIME HISTORY	YES	YES
AUTO-CORRELATION	YES	YES
CROSS-CORRELATION	YES	YES
PROBABILITY DENSITY	YES	YES
PEAK PROBABILITY DENSITY	YES	YES
STATISTICAL ACCURACY (BT PRODUCT)	64	64 (DATA DEPENDENT)
COMPUTER PRECISION	32 BITS FLOATING POINT	32 BITS FLOATING POINT
EDIT CAPABILITY	12 CHANNELS	12 CHANNELS
THROUGHPUT	N.D.	7.6 TIMES 704/ARP
RECURRING PERSONNEL SUPPORT	N.D.	-
SYSTEM HARDWARE COST	N.D.	-
SYSTEM INSTALLATION AND CHECKOUT COST	N.D.	\$807,640
SOFTWARE DEVELOPMENT COST	N.D.	7.6 PERSON YEARS

N.D. = GOAL NOT DECLARED

NOTE: REFER TO APPENDIX A FOR DETAILS OF PROJECTED PERFORMANCE.

TABLE 4
 DISPLAY PROCESS
 GOALS AND REQUIREMENTS VERSUS PROJECTED PERFORMANCE
 OF RECOMMENDED DISPLAY SYSTEM

STANDARD	GOAL	PROJECTED PERFORMANCE
THROUGHPUT	.5 8-1/2 x 11" PLOTS/SEC	1/2 PLOT/SEC
RESOLUTION (DOTS PER INCH)	160	200
CHOICE OF FORMATS	STANDARD CALCOMP	CALCOMP COMPATIBLE
RECURRING PERSONNEL	N.D.	-
SYSTEM HARDWARE COST	N.D.	-
SYSTEM INSTALLATION AND CHECKOUT COST	N.D.	\$68,700 TOTAL
SOFTWARE DEVELOPMENT COST	N.D.	.8 PERSON YEARS

- (2) Anti-alias filter size and complexity versus sample rate.
- (3) Analog versus digital filter implementation.
- (4) Establishment of recorder bit rate and storage requirements and capabilities.
- (5) Channel and bandwidth capacity versus recording time for stationary and non-stationary acquisition modes.
- (6) Methods of encoding gain status of auto-range signal conditioners.
- (7) Phase matching in acquisition versus phase correction in analysis.
- (8) Data validation (quick-look) at test site.
- (9) Signal conditioning, including automatic gain ranging.
- (10) Sampling and A/D conversion, including sample and hold.
- (11) Transient response of filters.
- (12) Buffer storage and formatting requirements.
- (13) System calibration.
- (14) Remote multiplexing concepts.
- (15) Airborne subsystem size, weight, modularity and power requirements.
- (16) Increased maximum array size for analysis.
- (17) Addition of floating point processing capability.
- (18) Software programming and support equipment requirements.
- (19) Improved plot resolution.
- (20) Data editing methods.
- (21) Merging of analyses from multiple filter data.
- (22) Addition of zoom transform and modal analysis capability.

Detailed discussion of these study areas is found in Appendix C.

Airborne system features were selected as follows for all the system candidates based upon results of the above study areas.

- ° Data Compression for Stationary Acquisition -

Multiple low-pass encoding was found to be superior to a multiple bandpass (zoom) approach to compression. A configuration employing up to six lowpass filter functions per measurand was selected. Filter cutoff frequencies are 19.5 Hz to 20 KHz in two-octave increments.

- ° Data Sampling and Encoding -

For reasons of accuracy and inter-channel phase error, a dedicated sample and hold amplifier and 12-bit A/D should be used for each measurand channel.

- ° Encoder/Formatter System Architecture -

A distributed system employing remote encoding was chosen for reasons of modularity and flexibility. A parallel bus structure was selected because of the high data rates involved. For convenience in setup, the central control unit should employ removable erasable - PROM memory modules.

- ° Data Recording -

Two 28-track tape recorders are required with 1 7/8 to 120 ips speed range and a 10 1/2-inch reel size. (A single 28-track recorder with 3 3/4 to 240 ips speed range and a 14-inch reel size would also be sufficient; however, currently available airborne recorders do not go to 240 ips). Serial recording was chosen for reliability reasons and to conform to IRIG standards. Because of the high bit densities on tape, the randomized NRZ-Level (RNRZ-L) PCM code was chosen.

The ground system was found to require a floating point array processor and more memory than the existing AFWAL/FIBG system. Editing could be either manual or automated.

Three airborne system candidates and two ground system candidates are defined in Appendix D. These were evaluated to determine the final recommended system configuration.

5. SYSTEM CANDIDATES EVALUATION - AIRBORNE AND GROUND

The three airborne system candidates were based on alternate

methods of low-pass filter implementation. Two approaches employing switched-capacitor filters were rejected because of deficiencies in currently available filters. The recommended system employs four active, analog lowpass filters per measurand, plus a time-shared finite impulse response (FIR) digital filter system providing the two lowest cutoff frequency filter functions (Figure 5).

The two ground computer system candidates were based on 16-bit and 32-bit minicomputers. Twelve specific 16-bit systems (basic candidate) and 19 specific 32-bit systems (high-capacity candidates) were evaluated.

It was determined that the performance of a new computer system (as measured by a performance model defined in Appendix E) is required to be at least six times that of AFWAL/FIBG's current system. This eliminated the 16-bit (basic) candidate systems from consideration. Therefore, the recommended ground system utilizes a 32-bit minicomputer and an array processor.

Details of the airborne system and ground system candidates evaluation are found in Appendix E (Phase III Interim Report). Performance evaluation of the selected systems is summarized in Tables 2, 3, and 4.

SECTION V

CONCLUSIONS - RECOMMENDED SYSTEM DESIGN

The system design presented herein achieves the principal goals established in the study, including:

- ° 144 simultaneously acquired 20 KHz measurand channels;
- ° Up to 8 hours record time;
- ° 66 DB dynamic range;
- ° Ground data processing system commensurate with the capabilities of the airborne acquisition system.

The airborne acquisition system does not meet the goals for power, weight, and size - this is considered by MCAIR to be a necessary consequence of using currently available technology to meet the principal goals.

1. AIRBORNE PCM ACQUISITION/RECORDING, REPRODUCING AND DECOMMUNICATION

An overall view of the recommended system from transducer interface through PCM decommutation is shown in Figure 3. The airborne system features distributed architecture with up to nine 16-channel remote encoding modules to handle 144 transducer inputs. Communication to/from the central control unit is via a 16-bit parallel bus. The rate on each of the 16 lines is approximately 10 MHz in order to handle the maximum overall data rate (approximately 154 megabits per second) plus overhead.

Two Sangamo Sabre XII tape recorders are shown with their respective record electronics housing modules (two for each recorder). The PCM code employed is the RNRZ-L recommended in IRIG 106-80. The tape packing density resulting from the maximum bit rate is 26.8 kilobits per inch. The reproducer is an existing AFWAL/FIBG Honeywell 96C modified for 28-track wideband (2 MHz at 120 ips) direct reproduce capability. (This modification consists of new heads and additional preamplifiers.) The reproduced data is still randomized at this point since bit synchronization is required prior to derandomizing.

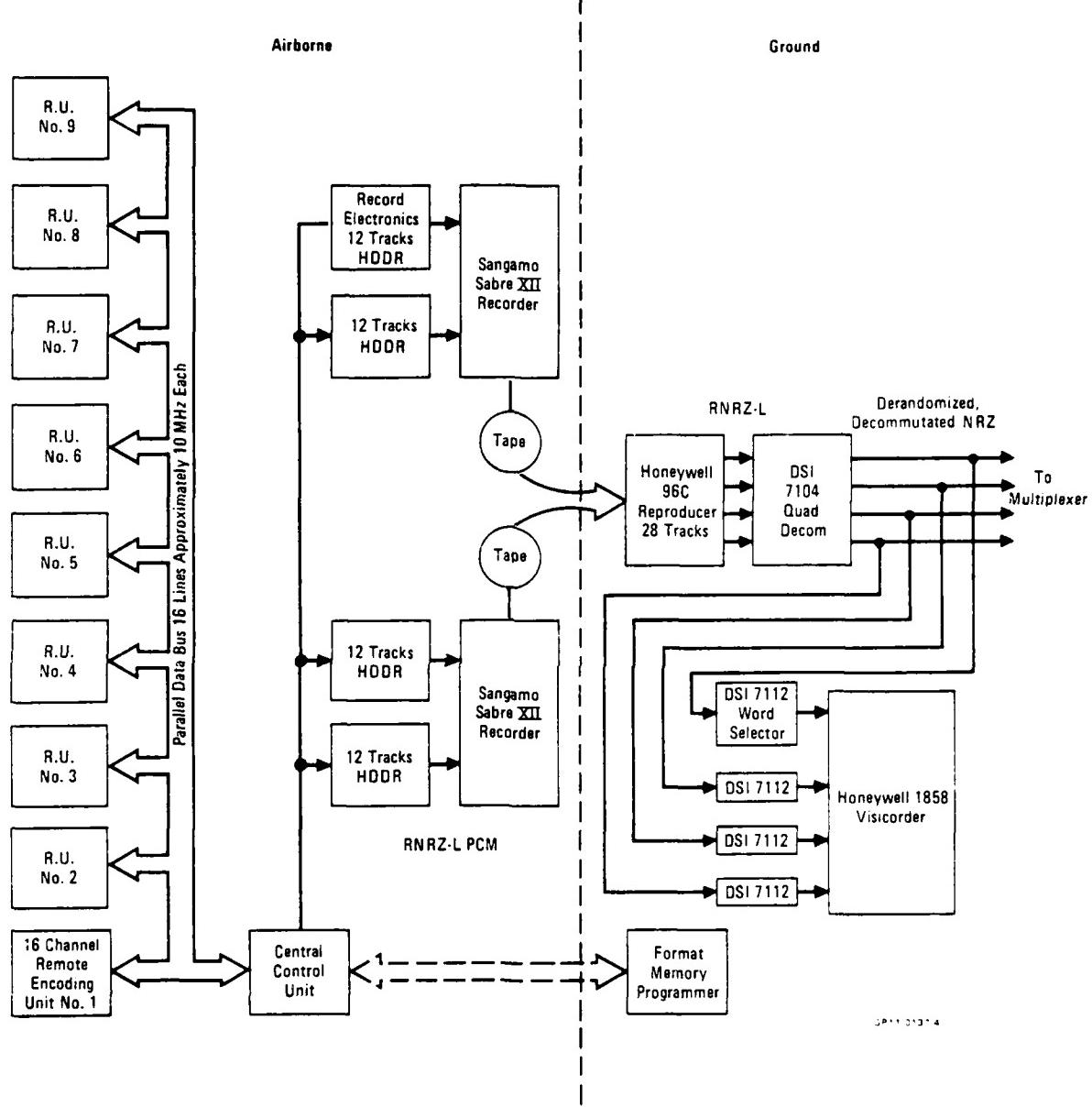


FIGURE 3
RECOMMENDED SYSTEM - AIRBORNE PCM ACQUISITION/RECORDING,
REPRODUCING AND DECOMMUTATION

Power, weight, and size of the airborne modules are indicated below. Information about the PCM modules is based on design studies by SCI Systems, Incorporated included in Appendixes C, D, and E. Information about the Sangamo tape recorders was taken from vendor literature, dated April 1979.

PCM Remote Unit:

- ° 81.9 watts (including dissipation in 70% efficient internal power supply)
- ° 24.01 lbs
- ° 0.437 cubic feet (9.75" W x 8.38" H x 9.25" L, including .5" cooling fins spaced approximately .45" apart)

PCM Central Unit:

- ° 95 watts (including dissipation in 70% efficient internal power supply)
- ° 23.34 lbs
- ° 0.437 cubic feet (same dimensions and fin design as remote unit)

Tape Transport (Including Tape and Shock Mounts):

- ° 150 watts
- ° 49 lbs
- ° 1.11 cubic feet (18.75" x 12.25" x 8.375")

Record Electronics Housing:

- ° 60 watts
- ° 10 lbs
- ° 0.31 cubic feet (7.5" x 7.5" x 9.5")

Since at the maximum response, only three measurands can be recorded per tape track, simultaneous decommutation of four tracks is required to meet the goal of editing 12 measurands per pass over the tape. A DSI 7104 quad decom was selected for this purpose. This is compatible with the DSI multiplexer used in the ground computer system (Figure 10) and it also contains a derandomizer required to decode the RNRZ-L. For manual editing via AFWAL/

FIBG's existing Honeywell Visicorder, DSI 7112 word selectors (including D/A converters) are shown.

Figure 4 is a block diagram of the PCM encoder/formatter system, showing details of both the central and remote units. Calibration switches are shown so that an external stimulus can be applied to all data channels of a remote unit for a system throughput calibration. Signal conditioning amplifiers feature automatic gain ranging with eight gain levels. A monolithic sample and hold circuit (50-nsec aperture and .16 watts per channel) is provided to minimize inter-channel phase errors. A 12-bit successive approximation A/D (32-pin hybrid module) is employed for each data channel. It consumes 1.2 watts and has a 5-microsecond conversion time. Communication to/from the central unit is via a 16-bit parallel data bus. The data bus interface in each module dissipates 9.5 watts. The central unit contains a large data buffer memory to smooth out the varying sample rates (from the different filters) to a constant rate to the tape recorder interface. The data buffer memory is over a million 16-bit words (see Appendix C, page 179). The tape recorder interface provides NRZ-L PCM data in up to 48 separate streams. Conversion to RNRZ-L is done in the tape recorder electronics.

Figure 5 shows the recommended arrangement of six lowpass filter functions per measurand. The four highest cutoff frequency filters (312.5 Hz - 20 KHz) are active analog filters located in the remote unit. One set of four such filters is dedicated to each measurand. The characteristics are Type I Chebyshev [12], designed for 0.1 dB peak-to-peak passband ripple. Cutoff frequency is defined as the highest -.1 dB point, referenced to the DC gain. Filters of like cutoff frequency for the various measurands must be adjusted during manufacture, for matching passband phase characteristics ($\pm 3^\circ$ over the temperature range). The remaining two lowest cutoff frequency filter functions are provided by a time-shared FIR digital filter system, located in the central unit. In Appendix C, this combination of high frequency analog and low frequency digital filters is shown to be optimum for this application. Appendix C also contains a listing of FIR filter weights computed for this

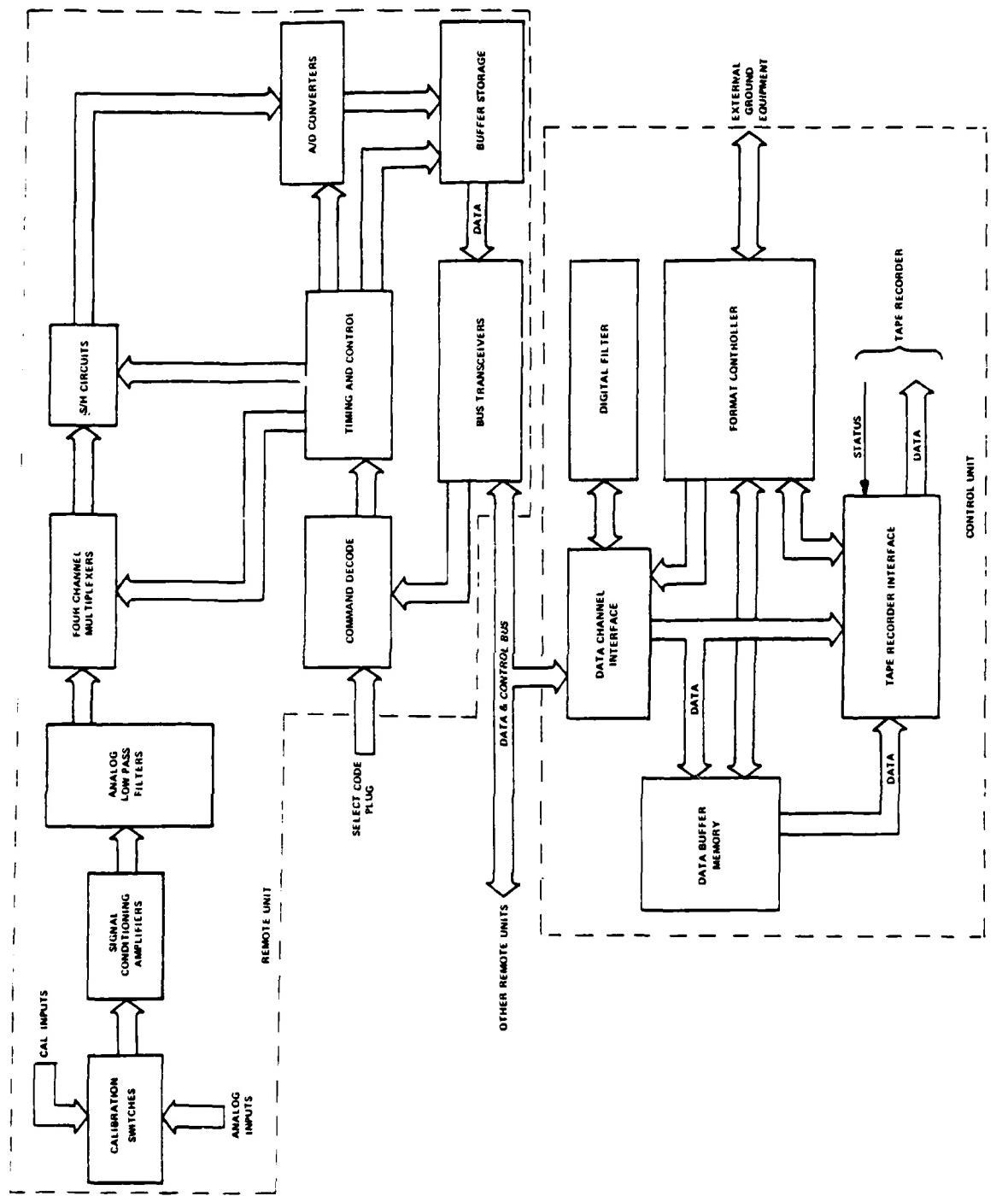


FIGURE 4
BLOCK DIAGRAM - PCM ENCODER/FORMATTER SYSTEM

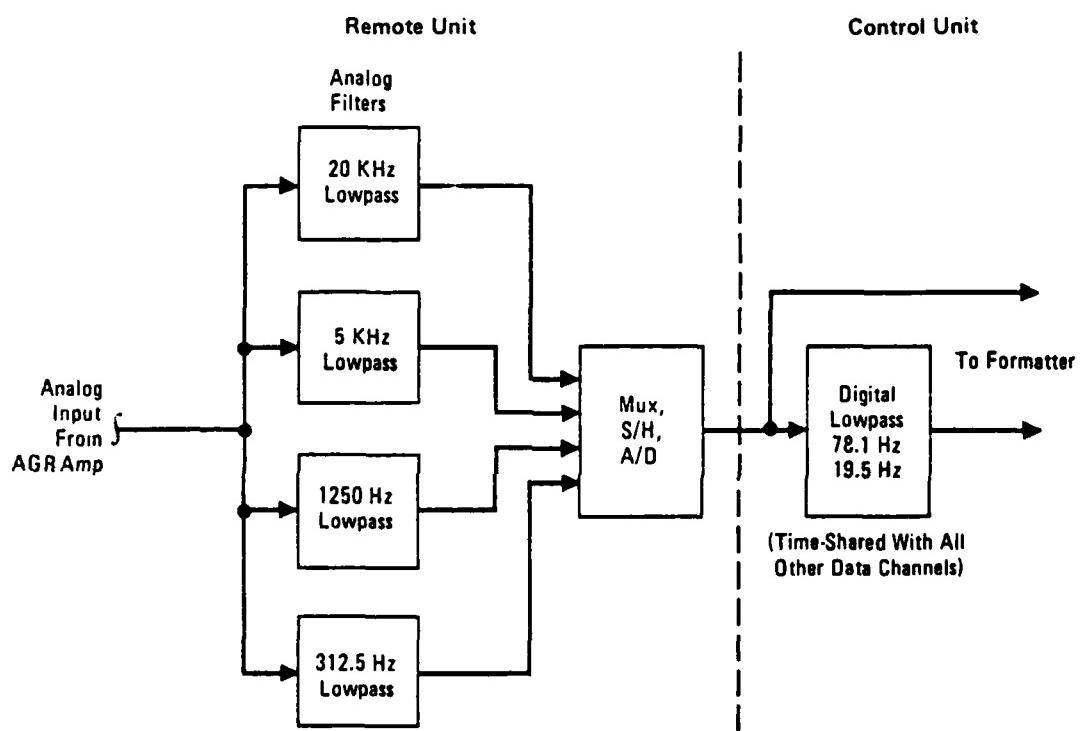


FIGURE 5
BLOCK DIAGRAM - RECOMMENDED FILTER CONFIGURATION

application. A 16-bit digital multiplier is required to implement the digital filters.

Table 5 summarizes important features and characteristics of the airborne acquisition and recording system, for three principal (20 KHz) operating modes. Mode A, which is suitable for either transient or stationary data, employs continuous sampling at 65,536 samples per second for each measurand, using the 20-KHz filter. Because of the high bit rate involved, the tape speed must be 120 ips, thus limiting the record time to 7.5 minutes (based on a 10 1/2 inch diameter tape reel containing 4600 feet of tape). Modes B and C, which are suitable for stationary data only, feature multiple filter encoding for data compression so that the recorder(s) can be slowed down to 1 7/8 ips to achieve 8 hours record time. Mode B, which employs all six filters, has the highest compression ratio, and allows 144 measurands to be recorded on only 24 data tracks, using a single 28-track recorder. Mode C requires two recorders, but it has a much lower "time update" (time to scan once through all filters, which is proportional to the number of samples per filter per update) so that stationary record length requirements are 1/4 that of Mode B.

Figures 6 and 7 show the recommended 392-word format structures for Modes A and C, and Mode B, respectively. Two 16-bit words each are allocated for frame synchronization, frame count, and time code. Word number 7 is a data status word used to identify the particular filter the data is coming from and the filter sample set (see details in Figure 8). One unused (spare overhead) word has been allocated; thus, there are a total of eight overhead words. The remaining 384 words in the frame are data words (shown in Figures 6 and 7 as M_{ij} , where i = measurand number and j = sample number within the sample set of a frame). There are 128 data samples per measurand in each frame for Modes A and C, and 64 samples per measurand for Mode B. The recommended 16-bit data word structure is shown in Figure 9. Each word contains three bits of gain code and 12 bits of data.

Refer to Tables A-9 and A-10 (pp.81-84) for the estimated cost breakout (non-recurring and recurring) for the development of the recommended airborne system.

SUMMARY OF AIRBORNE SYSTEM DESIGN FEATURES AND CHARACTERISTICS

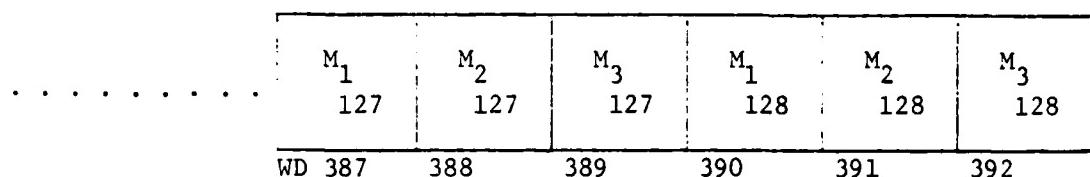
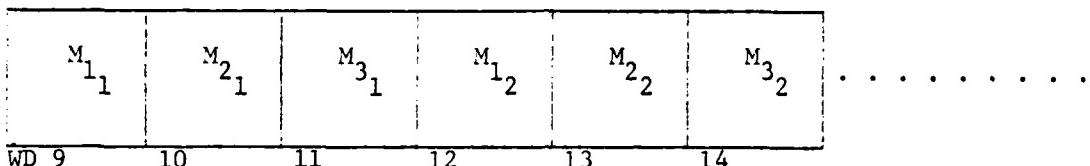
	MODE A (TRANSIENT OR STATIONARY)	MODE B (STATIONARY)	MODE C (STATIONARY)
TOTAL NO. OF MEASURANDS	144	144	144
FREQUENCY RANGE	DC - 20 KHZ	DC - 20 KHZ	DC - 20 KHZ
TIME UPDATE	N/A	2.67 - 42.6 SEC*	0.67 - 10.66 SEC*
TOTAL RECORD TIME	7.5 MINUTES	8 HOURS	8 HOURS
NO. OF FILTERS SAMPLED	1	6	5
FILTER CUTOFF FREQUENCIES	20 KHZ	19.5 HZ TO 20 KHZ (TWO OCTAVE STEPS)	78.1 HZ TO 20 KHZ (TWO OCTAVE STEPS)
SAMPLES PER CYCLE	3.2768	3.2768	3.2768
SAMPLE RATE COMPRESSION RATIO	1	227.5	68.2
SAMPLES PER FILTER PER UPDATE	N/A	128 TO 2048	128 TO 2048
ENCODING RESOLUTION	12 BITS	12 BITS	12 BITS
AUTORANGE	3 BITS (8 STEPS)	3 BITS (8 STEPS)	3 BITS (8 STEPS)
NO. OF MEASURANDS PER TAPE TRACK	3	6	3
NO. OF BITS PER WORD	16	16	16
NO. OF WORDS PER PCM FRAME	392	392	392
FRAME RATE	512/SEC	4.501099/SEC	7.5073313/SEC
BIT RATE PER TRACK	3.21 MEGABITS/SEC	28.2 K11.0BITS/SEC	47.09 KILOBITS/SEC
TAPE SPEED	120 I.P.S.	1 7/8 I.P.S.	1 7/8 I.P.S.
BIT PACKING DENSITY	26.8 KILOBITS/INCH	15.1 KILOBITS/INCH	25.1 KILOBITS/INCH
PCM CODE	RNRZ-L	RNRZ-L	RNRZ-L
NO. OF TAPE TRACKS	48	24	48

* (PROPORTIONAL TO SAMPLES PER FILTER PER UPDATE)

WORDS 1 THRU 8 (ALL 16 BIT WORDS)

SYNC WD 1	SYNC WD 2	FRAME COUNT WD 1	FRAME COUNT WD 2	TIME CODE MSW	TIME CODE LSW	DATA STATUS	SPARE
--------------	--------------	------------------------	------------------------	---------------------	---------------------	----------------	-------

WORDS 9 THRU 392 (ALL 16 BIT WORDS)



FORMAT CHARACTERISTICS	MODE	
	A	C
° COMPRESSION RATIO	1	68.2
° MEASURANDS/FRAME	3	3
° WORDS/FRAME	392	392
° BITS/WORD	16	16
° FRAMES/SECOND	512	7.507

FIGURE 6
RECOMMENDED PCM FORMAT STRUCTURE
MODE A OR C

WORDS 1 THRU 8 (ALL 16 BIT WORDS)

SYNC WD 1	SYNC WD 2	FRAME COUNT WD1	FRAME COUNT WD 2	TIME CODE MSW	TIME CODE LSW	DATA STATUS	SPARE
--------------	--------------	-----------------------	------------------------	---------------------	---------------------	----------------	-------

WORDS 9 THRU 392 (ALL 16 BIT WORDS)

M ₁ 1	M ₂ 1	M ₃ 1	M ₄ 1	M ₅ 1	M ₆ 1	M ₁ 2	M ₂ 2	M ₃ 2	M ₄ 2	M ₅ 2	M ₆ 2
WD 9	10	11	12	13	14	15	16	17	18	19	20
.....
.....
.....

M ₁ 127	M ₂ 127	M ₃ 127	M ₄ 127	M ₅ 127	M ₆ 127	M ₁ 127	M ₂ 128	M ₃ 128	M ₄ 128	M ₅ 128	M ₆ 128	
WD	382	384	386	388	390	392						
.....
.....
.....

MODE

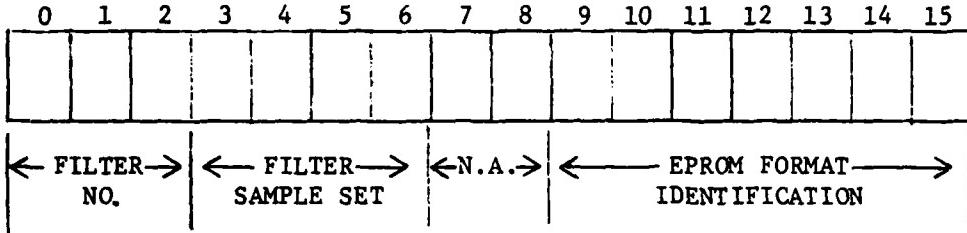
B

FORMAT CHARACTERISTICS

- COMPRESSION RATIO 227.5
- MEASURANDS / FRAME 6
- WORDS / FRAME 392
- BITS / WORD 16
- FRAMES / SECOND 4.501

FIGURE 7
RECOMMENDED PCM FORMAT STRUCTURE
MODE B

BIT
NO.



<u>FILTER NO.</u>	<u>STATUS WORD CODE</u>	<u>FILTER CUTOFF FREQUENCY</u>
0	0 0 0	20 KHZ
1	0 0 1	5 KHZ
2	0 1 0	1250 HZ
3	0 1 1	312.5 HZ
4	1 0 0	78.1 HZ
5	1 0 1	19.5 HZ
UNDEFINED	1 1 0	
UNDEFINED	1 1 1	

- FILTER SAMPLE SET - SYSTEM MAY BE FORMATTED TO ACCOMMODATE FROM 2^7 TO 2^{11} SAMPLES PER FILTER AND EACH PCM FRAME SUPPORTS A MAXIMUM OF 2^7 SAMPLES PER MEASURAND, HENCE THIS FIELD IS REQUIRED TO DESIGNATE THE SPECIFIC SAMPLE SET PER FILTER AS FOLLOWS:

<u>CODE</u>	<u>SAMPLE SET</u>
0 0 0 0	1 THRU 128
0 0 0 1	129 THRU 256
0 0 1 0	257 THRU 384
0 0 1 1	385 THRU 512
.	
.	
.	
1 1 1 1	1921 THRU 2048 (LIMIT SAMPLES/FILTER)

- N.A. IS NOT ASSIGNED

FIGURE 8
RECOMMENDED DATA STATUS WORD STRUCTURE

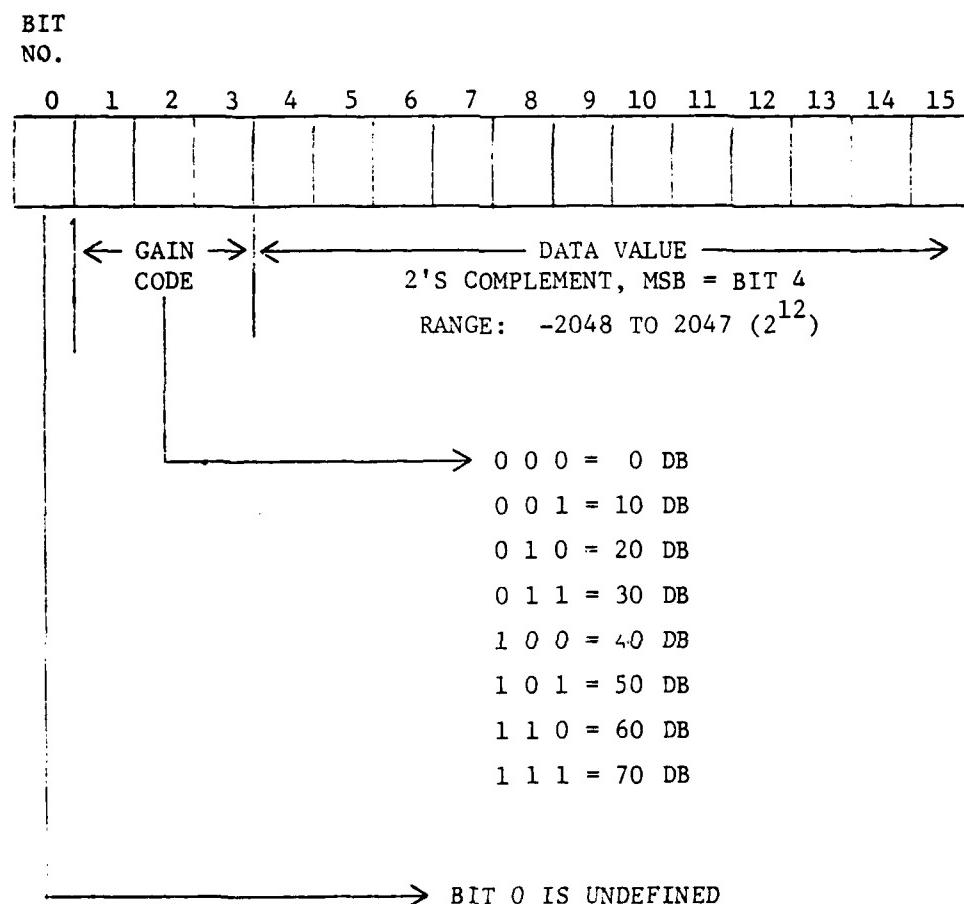


FIGURE 9
RECOMMENDED DATA WORD STRUCTURE

2. GROUND ANALYSIS AND DISPLAY SYSTEM

Figure 10 shows the recommended ground system from decom multiplexer through data plotters. Major components of the system are a Digital Equipment Corporation VAX 11/780 host computer and a Floating Point Systems AP-180V array processor. The FPS AP-180V is a modified AP-120B which realizes 5.5 megabytes per second (MB/S) for the array processor to host bus interface rate (APBIR) using a VAX 11/780 as host. This is the highest APBIR available in the market place, although it is lower than the 8.1 MB/S projected during Phase III of the study. Thus, the performance of the system (as measured by the performance model defined in Appendix E) is 11.71 (instead of 12.84 as reported at the end of Phase III). Appendix E showed that a minimum performance of 9.24 is required for the new system. Therefore, the DEC/FPS system is still deemed adequate for the application.

However, the computer market place continues to change at a rapid pace. Since the end of September 1980, DEC has announced price increases (roughly 5%), and Harris and FPS have developed a 3.2 MB/S APBIR interface for the Harris 800 computer, resulting in an increase in performance at no additional cost for the Harris/FPS system. Table 6 and Figure 11 summarize performance and cost for the high capacity (32 bit minicomputer) system candidates. These illustrations replace the Phase III summary (Appendix E, Figure E-19 and Table E-20). Figure 12 is a summary of performance and cost for those candidates that meet or exceed the 9.24 performance index requirements. These figures show that now both the Harris 800 and the Perkin-Elmer 3240 systems are less costly alternatives to the DEC system, in terms of hardware capability as measured by the performance model. During Phase IV, development of procurement plans for the ground system proceeded on the basis of the DEC system since secondary factors defined by "multi-user support", "network potential", "broad software base", and "hardware and software maturity" were all strengths for DEC as shown in Table 7. In the computer marketplace the performance and cost of minicomputers will continue to change. Secondary factors for the Harris system, when compared to the more positive secondary factors for the DEC system

in Table 7, may also change as the Harris installation base grows.

Therefore, based on the DEC computer system, a two stage procurement plan is shown in Tables 8 and 9. Table 10 shows the performance figures for the system and components for both Stage I and Stage II. A rack layout and floor plan are shown in Figures 13 and 14, respectively. The ground system requires a room size of 26.5 feet by 20.5 feet. Table 11 summarizes the power and cooling requirements and weight for the ground system computer hardware. A cost summary is provided in Table 12. Tables 13 through 24 provide detailed model numbers, descriptions and 1980 prices for Stage I and Stage II procurements. Table 25 provides cost information for an optional word processing capability with the VAX 11/780 computer. The word processors may be located in another room in the same building or located in another building using modems and phone lines.

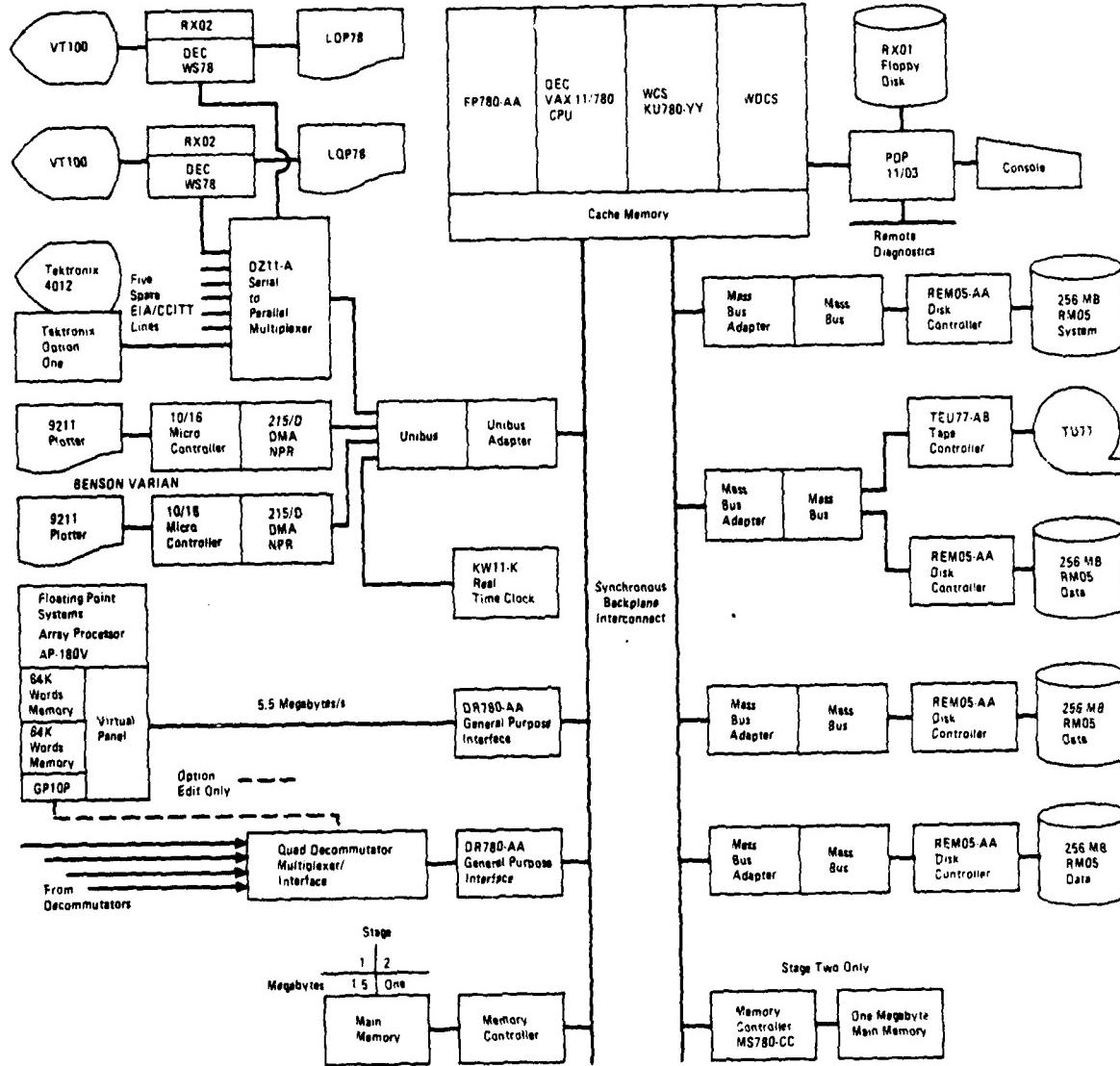


FIGURE 10
GROUND COMPUTER FACILITY BLOCK DIAGRAM

TABLE 6
BASIC AND HIGH CAPACITY HOST AND AP SYSTEM COST,
PERFORMANCE, P/C SUMMARY

MODEL	AP & HOST COST	P(HOST)	P/C (HOST)	P(HOST) + (P(AP)/5)	BASIC & AP K-1,000,000 10% CHG
DEC PDP 11/34A VA	\$711,925	1.47	11.73	3.5	16.52
DEC PDP 11/34A VB	230,225	1.66	11.56	3.69	16.03
DEC PDP 11/60 VA	245,175	1.66	10.47	3.69	15.05
DEC PDP 11/60 VB	263,475	1.85	10.46	3.88	14.73
DEC PDP 11/70 VA	295,275	2.38	11.41	4.41	14.94
DEC PDP 11/70 VB	334,175	3.26	13.17	5.29	15.83
DG ECLIPSE S/230 VA	293,200	2.92	14.10	4.95	16.88
DG ECLIPSE S/250 VB	298,400	3.09	14.55	5.12	17.16
DG ECLIPSE S/250 VC	303,200	3.34	15.38	5.37	17.71
DG ECLIPSE S/250 WD	308,400	3.50	15.74	5.53	17.93
HP 1000 (45) VA	216,070	1.96	15.32	3.99	18.47
HP 1000 (45) VB	228,070	2.50	17.86	4.53	19.86
DEC VAX 11/780 VA	535,695	7.44	18.25	10.69	19.96
DEC VAX 11/780 VB	639,695	9.59	18.74	12.84	20.07
PHASE IV STAGE I DEC VAX 11/780	534,770	6.74	12.60	9.26	17.35
*3 PHASE IV STAGE II DEC VAX 11/780	712,440	8.47	15.57	11.71	16.44
PE 3240 VA	450,995	7.13	22.17	10.38	23.02
PE 3240 VB	528,395	9.28	23.26	12.53	23.71
HARRIS 500 VA	452,770	3.78	11.69	7.03	15.53
HARRIS 500 VB	519,770	5.13	13.14	8.38	16.12
HARRIS 500 VC	531,340	5.82	14.48	9.07	17.07
*4 HARRIS 800 VA MODIFIED	518,845	6.13	15.74	9.38	18.08
*4 HARRIS 800 VB MODIFIED	585,845	7.48	16.39	10.73	18.31
*4 HARRIS 800 VC MODIFIED	597,415	8.17	17.46	11.42	19.11
*5 PHASE IV HARRIS 800 WD	668,675	9.19	17.04	12.44	18.61
MODCOMP 7870 VA	446,345	4.04	12.75	7.29	16.33
MODCOMP 7870 VB	539,195	6.19	15.11	9.44	17.51
PRIME 750 VA	454,445	4.93	15.17	8.18	18.00
PRIME 750 VB	540,445	7.26	17.66	10.51	19.45
DG MV/8000 VA	473,890	5.08	14.75	8.33	17.58
DG MV/8000 VB	539,190	7.02	17.13	10.27	19.05
*1 SEL 32/7780 VA	435,785	6.47	N/A *1	8.21	18.84
*1 SEL 32/7780 VB	511,750	8.29	N/A *1	10.03	19.60
*1 SEL 32/7780 VC	597,750	8.29	N/A *1	10.75	17.98
	*2)				

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

*1) NOT APPLICABLE SINCE P/C(HOST) FOR OTHERS DID NOT REFLECT ARRAY PROCESSOR PRICE.

*2) ASSUMES BASIC OR HIGH CAPACITY API24B EXCEPT IN SEL WHERE MAP 300 WAS CHOSEN.

*3) INSTALLATION COSTS INCLUDED IN STAGE II SO OTHER CANDIDATE P/C VALUES CANNOT BE COMPARED TO THE PHASE IV STAGE II VAX 11/780.

*4) APBIR CHANGED BETWEEN PHASE III AND PHASE IV UPGRAD.

*5) REQUIRED THIRD DATA DISK AND CONTROLLER ADDED TO HARRIS 800 VC MAKING A NEW CANDIDATE LABELED PHASE IV HARRIS 800 WD.

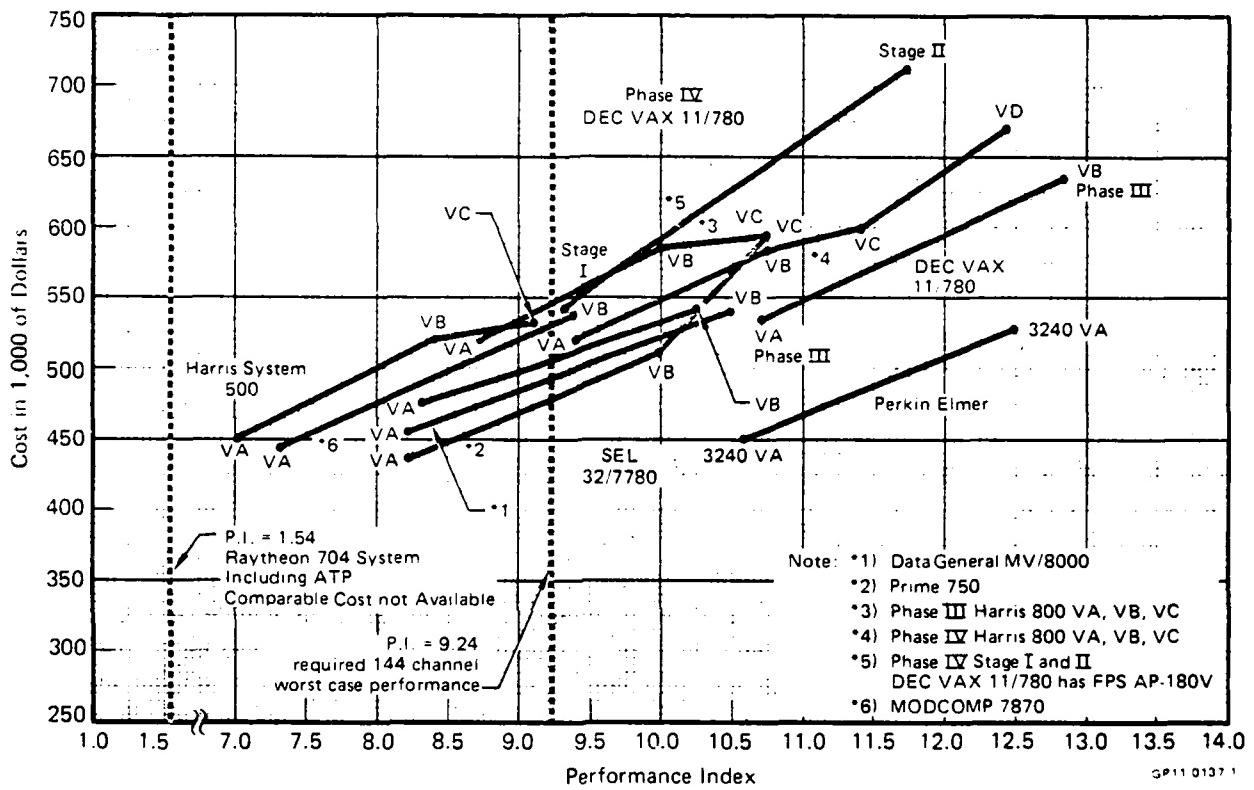


FIGURE 11
 HIGH CAPACITY SYSTEM COST
 vs PERFORMANCE INDEX
 (HOST and AP-120B)

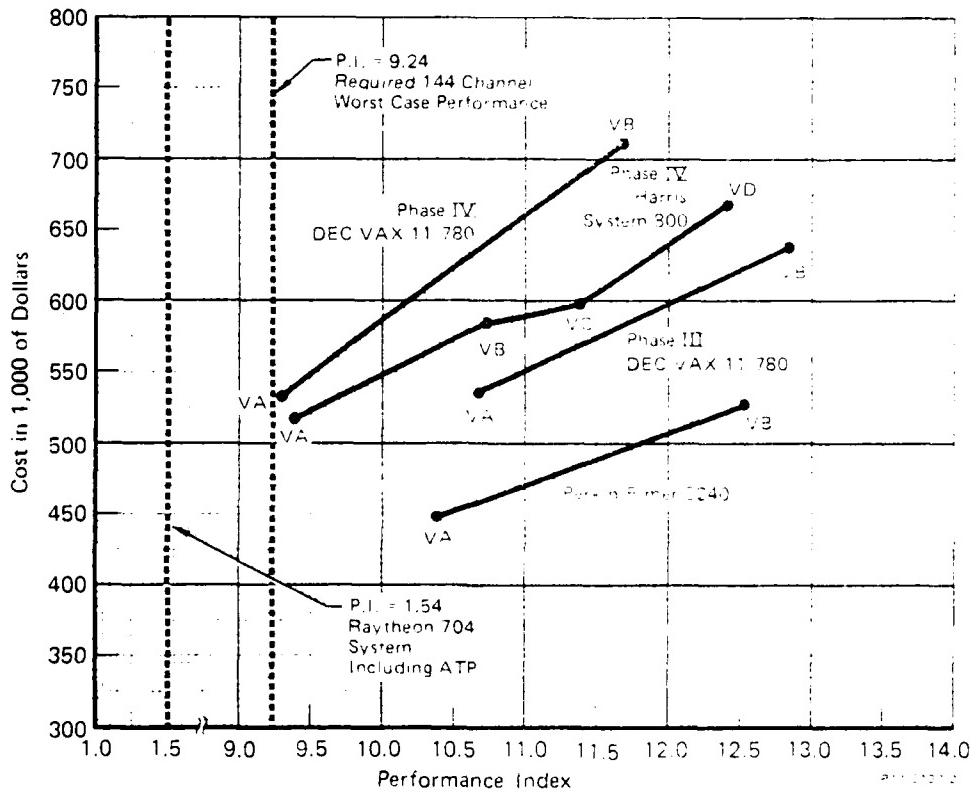


FIGURE 12
HIGH CAPACITY SYSTEM COST
vs PERFORMANCE INDEX
(HOST and AP-120B)

TABLE 7
DEC VAX, PE 3240, *HARRIS 800 COMPARISONS

DEC VAX <u>11/780</u>	PE 3240	HARRIS* SYSTEM 800
-----------------------------	------------	--------------------------

PRIMARY FACTORS IN SELECTION

° WORKLOAD CAPABILITIES	+	+	+
° PERFORMANCE VERSUS INITIAL COST	-	+	+
° GROWTH POTENTIAL	+	+	+

SECONDARY FACTORS IN SELECTION

° MULTI-USER SUPPORT	+	-	+
° NETWORK POTENTIAL	+	-	-
° BROAD SOFTWARE BASE	+	-	-
° HARDWARE AND SOFTWARE MATURITY	+	-	+

* UPDATED FROM PHASE III

TABLE 8
GROUND SYSTEM STAGE I PROCUREMENT PLAN

STAGE I

DIGITAL EQUIPMENT CORPORATION -

- VAX 11/780 TRAINING COURSES.
- VAX 11/780 COMPUTER WITH 1.5 MEGABYTES MEMORY, 8 KB CACHE, FLOATING POINT ACCELERATOR, USER REAL TIME CLOCK, 512 MEGABYTES FORMATTED DISKS, VMS OPERATING SYSTEM, FORTRAN, BLISS, AND DATATRIEVE

FLOATING POINT SYSTEMS -

- FPS AP-120B TRAINING COURSES
- FPS AP-180V ARRAY PROCESSOR WITH 64 K WORDS FAST MEMORY, SIGNAL PROCESSING LIBRARY, ADVANCED MATH LIBRARY, STANDARD LIBRARY, EXPANDED RAM MEMORY, EXPANDED PROGRAM SOURCE MEMORY, VMS DRIVER SOFTWARE

TEKTRONIX -

- RS232C INTERFACE FOR EXISTING 4012
- EASY GRAPHING SOFTWARE PACKAGE
- INTERACTIVE GRAPHING PACKAGE (ADVANCED)

BENSON VARIAN -

- BV 9211 ELECTROSTATIC PLOTTER, 2 I.P.S., 200 DOTS PER INCH, NPR DMA INTERFACE, SORTED VECTOR - RASTER INTELLIGENT CONTROLLER, GRAPHICS PLOTTING ROUTINES, CHARACTER GENERATOR, TEST CHARACTER DIAGNOSTIC UNIT, ROLL TAKE-UP REEL

HONEYWELL -

- MODIFICATION OF EXISTING AFWAL/FIBG MODEL 96C REPRODUCER TO INCLUDE 28 TRACK WIDEBAND HEADS, 3 ADDITIONAL QUAD PREAMPLIFIERS

DSI -

- MODEL 7104 QUAD DECOM, 7151-500 PRIORITY MULTIPLEXER, 736 TELEMETRY DATA CHANNEL COMPATIBLE WITH VAX DR780
- MODEL 7112 WORD SELECTORS AND DACS (DIGITAL TO ANALOG CONVERTERS)

TABLE 9
GROUND SYSTEM STAGE II PROCUREMENT PLAN

STAGE II

DIGITAL EQUIPMENT CORPORATION -

- ° 512 MEGABYTES FORMATTED DISKS, INTERLEAVED MEMORY CONTROLLER WITH 512 K BYTES MAIN MEMORY, 12 K BYTES USER WRITEABLE CONTROL STORE, BASIC PLUS II

FLOATING POINT SYSTEMS -

- ° 64 K WORDS FAST MEMORY, GENERAL PURPOSE INPUT/OUTPUT PROCESSOR

BENSON VARIAN -

- ° SAME STAGE I PLOTTER SYSTEM EXCEPT FOR GRAPHICS PLOTTING ROUTINES

TABLE 10
PERFORMANCE INDICES OF RECOMMENDED SYSTEM AND COMPONENTS
(DEC VAX 11/780 AND FPS AP-180V)

	STAGE I	STAGE II
HOST COMPUTER	6.74	8.47
ARRAY PROCESSOR	12.7	16.24
SYSTEM	9.28	11.71

FOR REFERENCE

RAYTHEON 704 ~ 1.25

RAYTHEON ATP ~ 1.44

SYSTEM ~ 1.54

NOTE: $(P.I.)_{SYSTEM} = (P.I.)_{HOST} + .2 (P.I.)_{AP}$

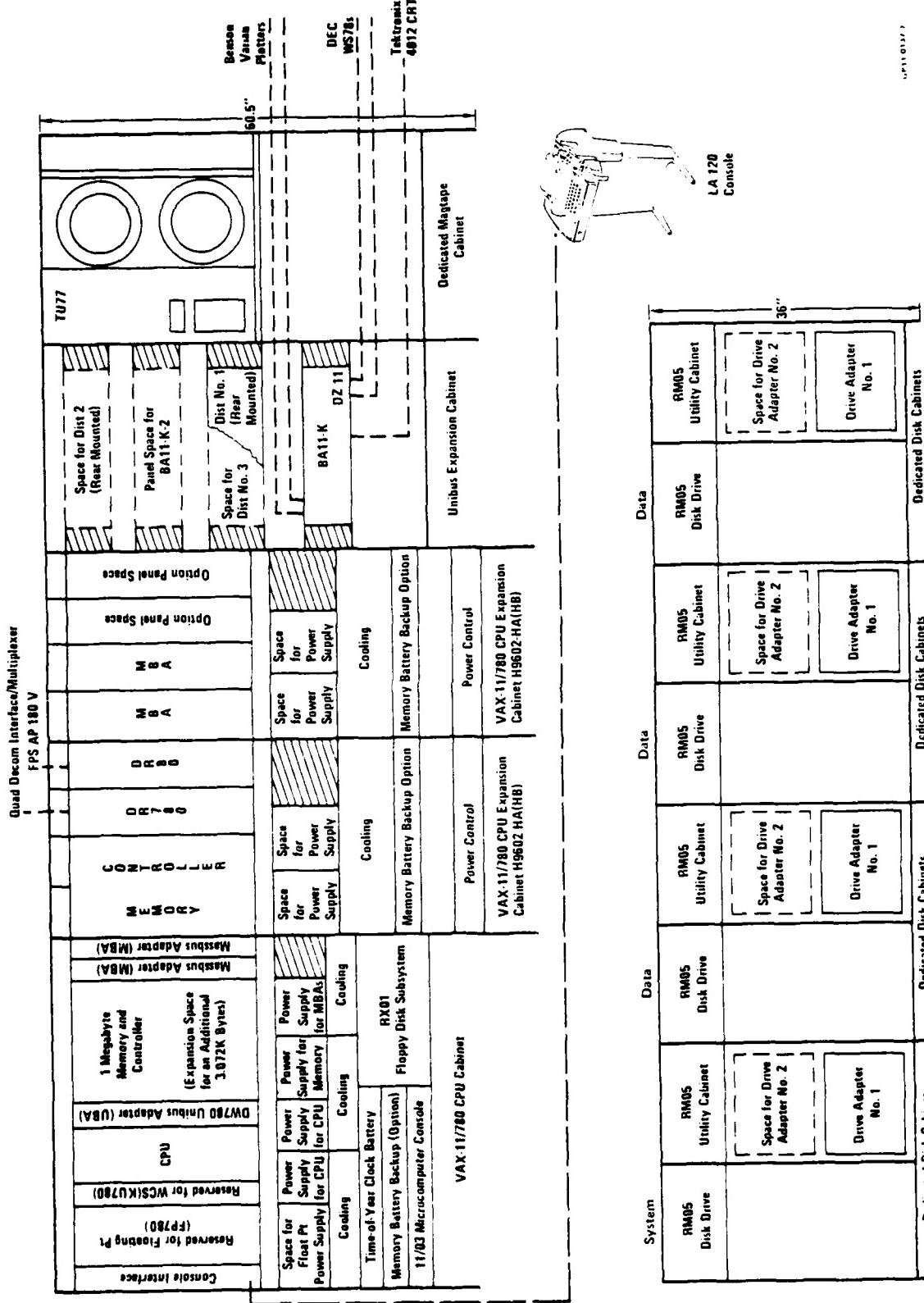


FIGURE 13
DIGITAL RMOS /VME77 BASED VAX-11/780 SYSTEM CONFIGURATION

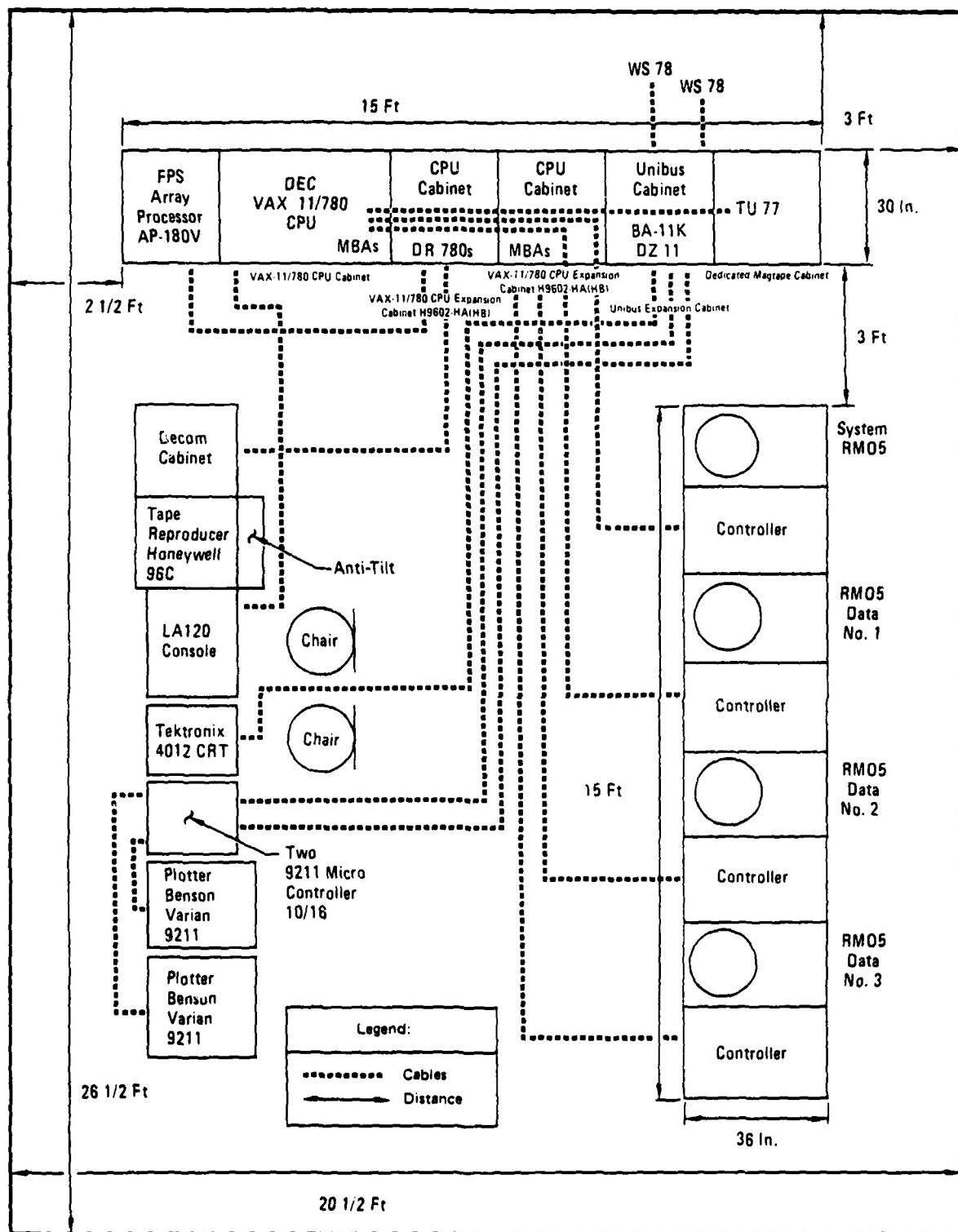


FIGURE 14
GROUND SYSTEM FLOOR PLAN

TABLE 11
POWER, COOLING, WEIGHT
GROUND COMPUTER SYSTEM

DESCRIPTION	POWER WATTS	COOLING BTUs/HR	WEIGHT LBS.
DEC VAX 11/780 COMPUTER SYSTEM	19,513	73,384	6,796
FPS AP-120B ARRAY PROCESSOR	1,800	~8,500	~250
BENSON VARIAN PLOTTER SYSTEMS (TWO)	890	3,038	740
TOTAL	22,203	84,922*	7,888

* NOTE: 500 BTU/HR PER PERSON IN SAME ROOM, SUNLIGHT EXPOSURE
INTO ROOM AND OTHER FACTORS INCREASE COOLING REQUIREMENTS

TABLE 12
GROUND SYSTEM COST SUMMARY

STAGE IA	DEC - VAX 11/780 TRAINING	\$ 12,450
IB	DEC - VAX 11/780 COMPUTER	407,690
IC	FPS - AP-120B TRAINING	1,650
ID	FPS - AP-180V ARRAY PROCESSOR	127,080
IE	TEKTRONIX - UPGRADE & GRAPHIC PACKAGES	8,085
IF	BV - PLOTTER SYSTEM	31,205
IG	HONEYWELL - TAPE REPRODUCER UPGRADE	10,000
IH	DSI - DECOM, MUX, INTERFACE, WORD SELECTORS AND DACS	71,100
Ii	APPLICATION SOFTWARE	6.2 PERSON YEARS
IJ	SYSTEM SOFTWARE	2.2 PERSON YEARS
		<hr/>
		\$669,260
STAGE IIA	DEC - VAX 11/780 UPGRADE	\$136,370
IIB	FPS - AP-180V UPGRADE	41,300
IIC	BV - PLOTTER SYSTEM	29,410
IID	GPIOP TO DECOM, EDIT ONLY OPTION	NQA
IIE	SYSTEM SOFTWARE FOR IID	NQA
		<hr/>
		\$207,080
		<hr/>
TOTAL STAGES I AND II		\$876,340 + 8.4 PERSON YEARS

NOTE: NQA - NO QUOTE AVAILABLE

STAGED GROUND FACILITY HARDWARE BREAKDOWN (TABLES 13 - 24)

TABLE 13
STAGE IA - DIGITAL EQUIPMENT CORPORATION

\$12,450 VAX TRAINING AT \$4,150 EACH, FOR 1 TO 3 PERSONS, 3 RECOMMENDED

- 1) VAX-11 INSTRUCTION SET
 - 2) VAX/VMS MACRO
 - 3) VAX/VMS FORTRAN IV MACRO PROGRAMMING
 - 4) VAX/VMS SYSTEM PROGRAMMER
 - 5) VAX/VMS DEVICE DRIVER
 - 6) VAX/VMS SYSTEM MANAGER
- 6 COURSES/PERSON
5 DAYS/COURSE
30 DAYS/PERSON
\$4,150/PERSON NOT INCLUDING TRAVEL EXPENSES OR LODGING

TABLE 14
STAGE IB - DIGITAL EQUIPMENT CORPORATION

SV-AXDBB-CA	VAX 11/780 CONFIGURATION WITH 1,536 KB MEMORY, 8 KB CACHE, 12 KB WRITABLE DIAGNOSTIC CONTROL STORE, REAL-TIME CLOCK, TIME OF YEAR CLOCK, 256 MB FORMATTED RM05 DISK DRIVE WITH CONTROLLER, FULLY SUPPORTED VAX/VMS	\$257,600
FP-780-AA	FLOATING POINT ACCELERATOR	10,600
(2) DR780-AA	SBI ADAPTER	37,400
KW11-K	REAL-TIME CLOCK	1,050
(2) H9602-HA	CPU EXPANSION CABINET	8,500
RM05-AA	RM05 DISK DRIVE	34,000
MD-VAX	DIAGNOSTIC SOURCE	3,000
MD-VAX-R	ONE YEAR DIAGNOSTIC UPDATE	1,800
ZE014-CY	USER DIAGNOSTIC SOURCE	1,150
QE001-MM	VMS SOURCE	25,000
QE106-AY	BLISS - 32 SYSTEM LANGUAGE	13,800
QE100-AY	FORTRAN IV PLUS LANGUAGE	7,000
QE105-AY	DATATRIEVE (DATA MANAGEMENT SERVICES)	4,500
BC06S-25	25 FT RM05 CONTROLLER CABLE	990
BC06S-40	40 FT RM05 CONTROLLER CABLE	1,300
		\$407,690

TABLE 15
STAGE IC - FLOATING POINT SYSTEMS

\$1,650 "AP-120B PROGRAMMING" TRAINING AT \$550 EACH, FOR 1
TO 3 PERSONS, 3 RECOMMENDED

1 COURSE/PERSON

5 DAYS/COURSE

5 DAYS/PERSON

\$550/PERSON NOT INCLUDING TRAVEL EXPENSES OR LODGING

TABLE 16
STAGE ID - FLOATING POINT SYSTEMS

AP-180V/064	AP180V CONFIGURATION WITH 64K WORDS 167 NS MEMORY	\$102,260
AP-PR/PG	PARITY AND PAGE SELECT	4,800
AP-SIGLIB	SIGNAL PROCESSING LIBRARY	975
AP-AMLLIB	ADVANCED MATH LIBRARY	500
AP-TMR	1 K WORDS RAM TABLE MEMORY	1,750
AP-TM16	2 K WORDS RAM TABLE MEMORY	1,650
SPECIFY	E1 BACKPLANE	
AP-PS2048	2K PROGRAM SOURCE MEMORY	7,145
AP-PDS	AP PROGRAM DEVELOPMENT SOFTWARE	3,000
AP-DE06-S	DEC VMS DRIVER	5,000
		\$127,080

TABLE 17
STAGE IE - TEKTRONIX

(4012) OPTION 1	RS232C INTERFACE	\$ 1,000	*1
*2 4010B01 - OPTION 33	EASY GRAPHING 9 TRACK, 800 BPI TAPE DOS FORMAT	1,900	
*2 4010C01 -	DEC VAX/VMS INTERACTIVE GRAPHING PACKAGE	5,185	
OPTION 2A	PRIMARY COMMAND SET AND MORTRAN		
3D AND 4D	GRAPHICS TEXT COMPOSER		
3E AND 4E	LINE SMOOTHING		
1A	4012 DEVICE DRIVER		
		\$ 8,085	

*1) NOTE: PLUS TRAVEL, EXPENSES, AND INSTALLATION

*2) NOTE: VMS PACKAGE SPECIAL ORDER, DO NOT SUBSTITUTE
RSX-11M DEVICE DRIVER

TABLE 18
STAGE IF - BENSON VARIAN

9211	ELECTROSTATIC PLOTTER 2 I.P.S., 200 DOTS PER INCH	\$ 14,000
* 903-13VMS	VAX 11/780 GRAPHICS PLOTTING ROUTINES (VMS DEVICE DRIVERS)	1,795
215/D	VAX 11/780 INTERFACE NPR	1,850
40-530	CHARACTER GENERATOR	1,110
40-781	ASCII TEST CHARACTER UNIT	350
10/16	GRAPHWARE 1 MICROPROGRAMMED CONTROLLER	10,950
40-172	ROLL TAKE UP REEL	1,150
		\$ 31,205

* NOTE: DO NOT SUBSTITUTE RSX11-M DEVICE DRIVERS

TABLE 19
STAGE IG - HONEYWELL

SPECIAL QUOTE	MODIFICATION OF EXISTING AFWAL/FIBG MODEL 96C REPRODUCER TO INCLUDE 28 TRACK WIDEBAND HEADS, 3 ADDITIONAL QUAD PREAMPLIFIERS	\$ 10,000
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TABLE 20
STAGE IH - DECOM SYSTEMS INCORPORATED

SPECIAL QUOTE	MODEL 7104 QUAD DECOM, 7151-500 PRIORITY MULTIPLEXER, 736 TELEMETRY DATA CHANNEL COMPATIBLE WITH VAX DR780	\$38,200
(4) DSI 7112	WORD SELECTORS AND DACS (DIGITAL TO ANALOG CONVERTERS)	32,900
		\$71,100

TABLE 21
STAGE IIA - DIGITAL EQUIPMENT CORPORATION

(2) REM05-AA	TWO RM05 DISK DRIVES AND CONTROLLERS- 256 FORMATTED MB EACH	\$ 90,484
MS780-CC	512 KB MEMORY WITH CONTROLLER	27,127
KU780-YY	USER WRITABLE CONTROL STORE - 12 KB	11,059
QE102-AY	BASIC PLUS II LANGUAGE	5,100
(2) BC06S-40	40 FT RM05 CONTROLLER CABLE	2,600
		\$136,370

TABLE 22
STAGE IIB - FLOATING POINT SYSTEMS

SP-DMF64	64K WORDS 167 NS MEMORY	\$ 34,000
* AP-GPIOP	GENERAL PURPOSE INPUT/OUTPUT PROCESSOR (INTERFACE): GPIOP	6,800
	FIELD ENGINEER INSTALLATION COSTS	500
		\$ 41,300

PLUS:

- ° BUS CONVERTER (GPIOP TO DECOM INTERFACE - EDIT ONLY OPTION)
- ° FIELD ENGINEER TRAVEL AND EXPENSES

* NOTE: IF EDIT ONLY OPTION NOT DONE, GPIOP TO DECOM, GPIOP IS NOT NEEDED.

TABLE 23
STAGE IIC - BENSON VARIAN

9211	ELECTROSTATIC PLOTTER 2 I.P.S., 200 DOTS PER INCH	\$ 14,000
215/D	VAX 11/780 INTERFACE NPR	1,850
40-530	CHARACTER GENERATOR	1,110
40-781	ASCII TEST CHARACTER UNIT	350
10/16	GRAPHWARE 1 MICROPROGRAMMED CONTROLLER	10,950
40-172	ROLL TAKE UP REEL	1,150
		\$ 29,410

TABLE 24
STAGE IID - NO QUOTES RECEIVED

*NO QUOTES RECEIVED	GPIOP FPS AP INTERFACE TO DECOM, EDIT ONLY OPTION
---------------------	---

*NOTE: THE ABOVE ITEM IS TECHNICALLY FEASIBLE BUT NOT AVAILABLE "OFF THE SHELF" STAGE IH FROM DSI SHOULD CONTAIN "HOOKS" FOR STAGE IID IF THE STAGE IID OPTIONAL THRUPUT ENHANCEMENT IS DONE.

TABLE 25
WORD PROCESSING CAPABILITY CONFIGURATION AND PRICE

STAGE WPI:

MODEL #	DESCRIPTION	PRICE
WS 78	VT100, RX02, AND LQP78 SINGLE USER WORD PROCESSING SYSTEM	\$ 7,795
	COMMUNICATIONS OPTION	\$ 1,050
QE707-YY	VAX 11/780 VMS COMMUNICATIONS SOFTWARE	\$ 2,900
		\$ 11,745

STAGE WPII:

MODEL #	DESCRIPTION	PRICE
WS 78	VT100, RX02, AND LQP78 SINGLE USER WORD PROCESSING SYSTEM	\$ 7,795
	COMMUNICATIONS OPTION	\$ 1,050
		\$ 8,845
	TWO USERS TOTAL	\$ 20,590

SECTION VI

RECOMMENDATIONS FOR FURTHER STUDY, DEVELOPMENT AND PROCUREMENT

This design study has resulted in a viable approach for developing an all PCM dynamic data system. However, the study was paced by stressing the principal requirements of bandwidth/measurand of DC to 20 KHz (\pm 1 dB) for 144 measurands. The study fulfilled these requirements while minimizing impact on remaining standards (Reference Table 2). Although the recommended system would serve AFWAL/FIBG objectives, further study is advisable in the following areas prior to proceeding with development. Specifically,

- (1) Secure a MIL-E-5400, Class 2 qualified tape recorder and ground reproducer which achieves the requirements of this study.
- (2) Evaluate advanced packaging technologies which may more closely achieve goals of power, weight, and size.
- (3) Evaluate selected computer/array processor systems with an AFWAL/FIBG benchmark program prior to final selection and procurement.
- (4) Develop an AFWAL/FIBG operational procedure for the recommended system, with respect to ground support facilities, for configuring and pre-test checkout of the system, both at AFWAL and the test site; and playback processing of acquired test data in the interest of maximizing test readiness while minimizing recurring personnel support.

Should AFWAL/FIBG decide to proceed with the proposed data system, then the recommended plan for development of the airborne and ground portions of the system is shown in Tables 26 through 31; 26 is a summary of milestone objectives and 27 is a summary of projected contract awards. This plan is ordered to minimize development risks and costs in the evolution of a fully qualified PCM dynamic data system. The following discussions will provide the rationale for this plan.

TABLE 26
MCAIR RECOMMENDED
AFWAL/FIBG DEVELOPMENT PLAN
SUMMARY

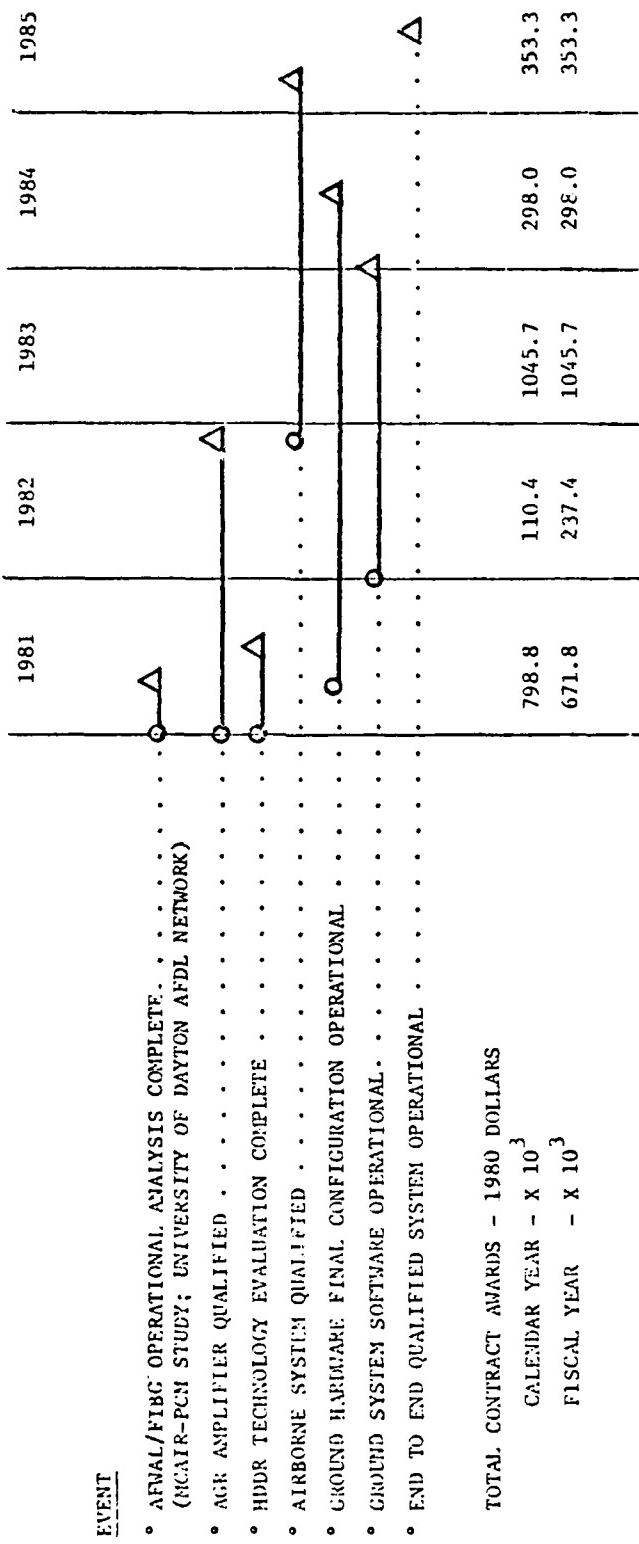


TABLE 27
 AFWAL/FIBG PCM SYSTEM
 SUMMARY OF PROJECTED CONTRACT AWARDS
 (BUDGETARY FIGURES, IN 1980 DOLLARS)

CALENDAR YEAR 1981

<u>VENDOR</u>	<u>ITEMS</u>	<u>\$ X 10³</u>
DEC	HOST COMPUTER STAGE I	407.7
FPS	ARRAY PROCESSOR STAGE I	127.1
DEC, FPS	TRAINING	14.1
TO BE DETERMINED	ACR AMPLIFIERS DEVELOPMENT	250.0
		1981 ~ 798.9

CALENDAR YEAR 1982

TEKTRONIX	INTERFACE FOR TERMINAL	8.1
BENSON VARIAN	PLOTTER	31.2
DSI	QUAD DECOM, MUX, BUS INTERFACE	38.2
DSI	4 WORD SELECTORS WITH D/A CONVERTERS	32.9
		1982 ~ 110.4

CALENDAR YEAR 1983

SCI	AIRBORNE ENCODER/FORMATTER SYSTEM DEV	868.0
DEC	HOST COMPUTER STAGE II	136.4
FPS	ARRAY PROCESSOR STAGE II	41.3
		1983 ~ 1045.7

CALENDAR YEAR 1984

SANGAMO	5 RECORDERS	269.9
SANGAMO	5 CONTROL UNITS (FLIGHT)	5.6
SANGAMO	2 CONTROL UNITS (GROUND)	4.5
SANGAMO	2 SCOPES	4.0
SANGAMO	5 DIRECT REPRODUCE AMP	1.6
SANGAMO	5 SETS OF EQUALIZERS	2.4
HONEYWELL	UPGRADE OF MODEL 96C	10.0
		1984 ~ 298.0

CALENDAR YEAR 1985

SCI	144 CHANNEL AIRBORNE SYSTEM	264.9
SCI	SUPPORT EQUIPMENT	59.0
BENSON-VARIAN	PLOTTER	29.4
		1985 ~ 353.3

TABLE 28
AFWAL/FIBG DEVELOPMENT PLAN
AIRBORNE SYSTEM

<u>EVENT</u>	1981	1982	1983	1984	1985
A. AUTO GAIN RANGING AMPLIFIER					
• ISSUE PROCUREMENT SPEC (AGR AMPLIFIER)	△				
• CONTRACT AWARD.	△				
• DEVELOPMENT AND QUALIFICATION TESTS COMPLETE.		△-△			
• ISSUE FINAL DOCUMENTATION		△-△			
• ISSUE PRODUCTION PROCUREMENT SPEC (AGR AMPLIFIER)			△		
• CONTRACT AWARD (PRODUCTION QUANTITIES)			△		
B. TAPE RECORD/REPRODUCE SYSTEM		△			
• HDDR TECHNOLOGY TEST AND EVALUATION COMPLETE.	△				
• ISSUE PROCUREMENT SPEC (GROUND UPDATE)		△			
• CONTRACT AWARD.		△			
• GROUND REPRODUCE UNIT OPERATIONAL			△		
• ISSUE PROCUREMENT SPEC (AIRBORNE UNITS)			△		
• CONTRACT AWARD.			△		
• UNITS NO. 1 AND 2 DELIVERED			△		
C. REMOTE AND CONTROL UNITS					
• ISSUE PROCUREMENT SPEC (REMOTE AND CONTROL UNITS)		△			
• CONTRACT AWARD.		△			
• BREADBOARD DEVELOPMENT AND DOCUMENTATION COMPLETE			△		
• PROTOTYPE TESTS COMPLETE.			△		
• QUALIFICATION UNITS TESTED.			△		
• SYSTEM INTEGRATION TEST COMPLETE.			△		
• ISSUE FINAL DOCUMENTATION			△		
• ISSUE PRODUCTION PROCUREMENT SPEC			△		
• CONTRACT AWARD (PRODUCTION QUANTITIES)			△		

TABLE 29
AFWAL/FIBG DEVELOPMENT PLAN
GROUND SYSTEM - HARDWARE

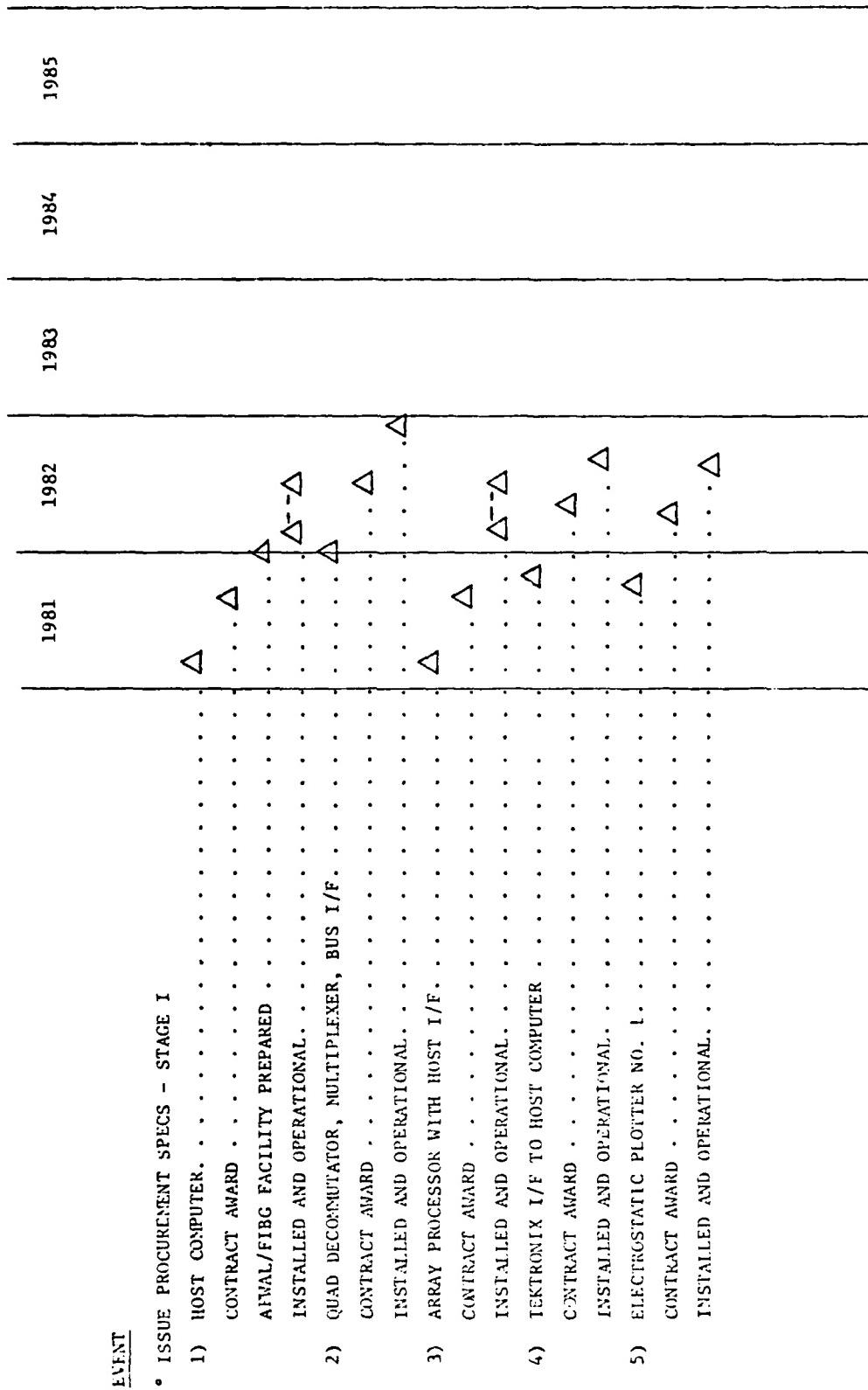
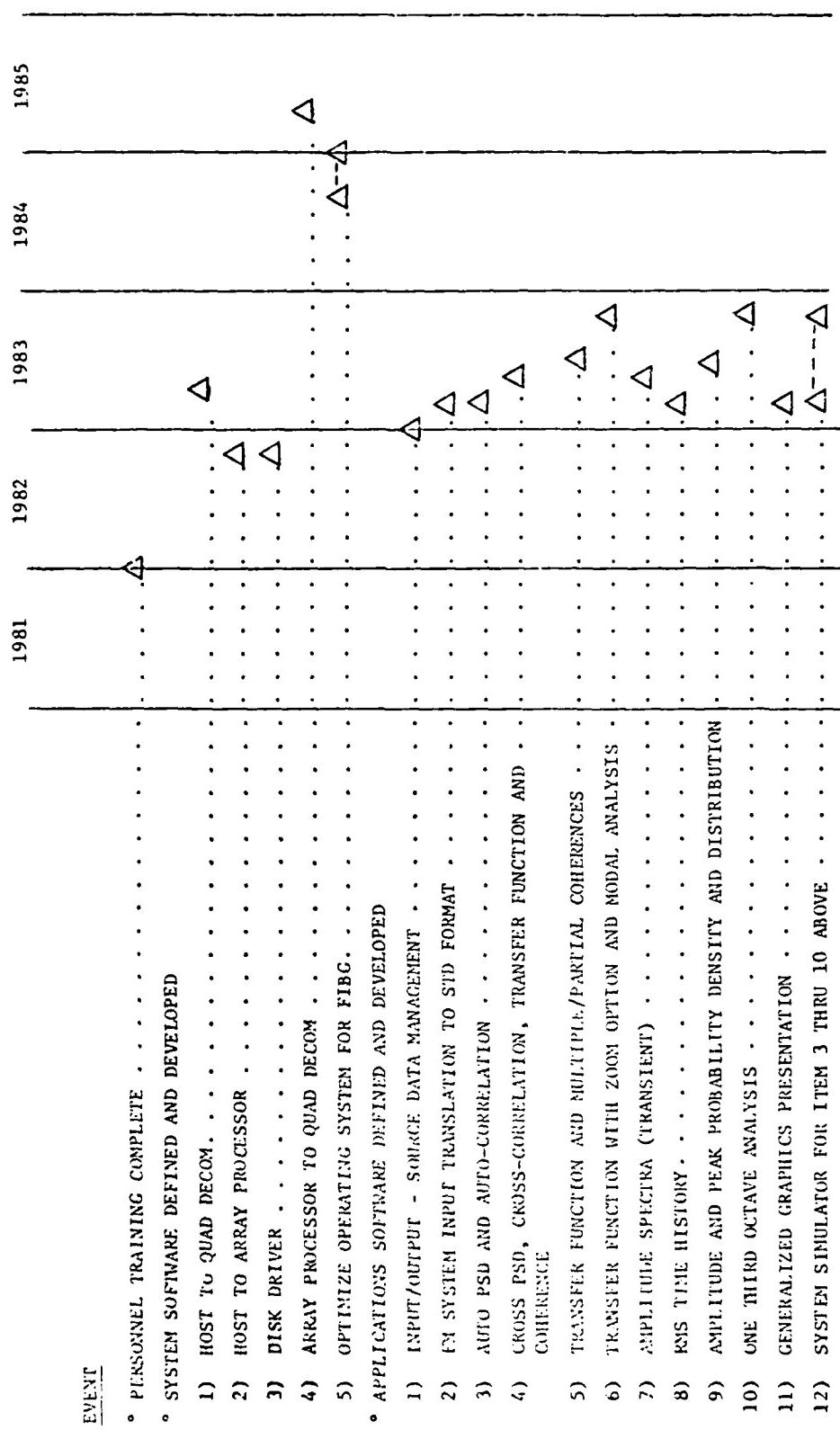


TABLE 30
AFWAL/FIBG DEVELOPMENT PLAN
GROUND SYSTEM - HARDWARE

EVENT	1981	1982	1983	1984	1985
• ISSUE PROCUREMENT SPECS - STAGE II					
1) HOST COMPUTER - FINAL CONFIGURATION
CONTRACT AWARD
INSTALLED AND OPERATIONAL
2) ARRAY PROCESSOR - FINAL CONFIGURATION
CONTRACT AWARD
INSTALLED AND OPERATIONAL
3) ELECTROSTATIC PLOTTER NO. 2
CONTRACT AWARD
INSTALLED AND OPERATIONAL

TABLE 31
AFWAL/FIBG DEVELOPMENT PLAN
GROUND SYSTEM - SOFTWARE



The ability of the system to achieve the required goals is predicated upon the performance claims of tape recorder manufacturers. Before commitment to development of the airborne system it is recommended that an investigation be conducted in the high density digital recorder technology. This recommendation is prompted by the fact that experimental knowledge is not available to substantiate performance claims by manufacturers (33.0 KBPI with BER $< 10^{-6}$) and no known applications of airborne recorders to the level demanded by design study exist (26.8 KBPI with BEP $< 10^{-6}$). This investigation is recommended to be performed by a qualified agency to evaluate the characteristics of errors for the operational range required by this study.

Since the automatic gain ranging amplifier could be employed by the existing as well as the proposed data system, it is recommended that development be initiated when AFWAL/FIBG deems practical. Further, it is considered advisable to secure a qualified amplifier design before issuing the procurement specifications for the proposed airborne system in order to avoid any specification changes induced from amplifier development (see Tables 26 and 28).

The proposed ground processing portion of the data system has been configured proportional to the bit rate potential of the proposed airborne system while maintaining approximately the same level of facility utilization as the existing Raytheon computer system. Tables 29 and 30 present the recommended ground system development plan which indicates a two stage procurement. When AFWAL decides to proceed, it is recommended that the Stage I procurement of the host computer, array transform processor, Tektronix interface, electrostatic plotter no. 1, and two word-processing stations (also used for software development) be initiated as denoted by Table 29. This portion of the ground system would support the processing requirements of the existing AFWAL FM airborne system while providing the support necessary for systems and application software development in preparation for the recommended airborne system. The quad PCM decommutator, multiplexer and Host bus interface must be deferred until commitment on proposed airborne system. The Stage II procurements are recommended to be

maintained in the same time relationship as development plan of the proposed airborne system in order to defer ground system costs until AFWAL forecast needs dictate.

APPENDIX A

BASIS OF PROJECTED PERFORMANCE OF RECOMMENDED SYSTEM DESIGN

This appendix contains design details and assumptions that are pertinent to the projected system performance summarized in Tables 2 and 3.

TABLE A-1
ERROR ANALYSIS - RECOMMENDED ACQUISITION SYSTEM

SOURCE OF ERROR	DC ERRORS OFFSET	GAIN	FREQUENCY RESPONSE ERRORS GAIN Δ	ALIASING ATTENUATION
			PHASE (INTER-CH.) Δ	
AGC AMPLIFIER	.63%	.01%	.05 dB	1.7°
ANALOG FILTERS	.02%	*	1 dB	2.4°
MULTIPLEXER	*	.01%	*	*
SAMPLE AND HOLD	.01%	*	.06 dB	.18°
A/D CONVERTER	.09%	.19%	*	*
DIGITAL FILTERS	*	*	.2 dB	*
OVERALL SYSTEM	R.S.S. .64%	R.S.S. .19%	R.S.S. 1.02 dB	R.S.S. 2.9°
	SUM .83%			66 dB

* = NOT APPLICABLE OR VIRTUALLY NO ERROR

Δ = DC TO 20 KHZ

Δ = MEASURED AT 10 KHZ

R.S.S. = ROOT-SUM-OF SQUARES COMBINATION OF ERRORS

TABLE A-2
REMOTE UNIT POWER, SIZE, RELIABILITY

<u>POWER</u>	<u>NO. OF 9" x 6.9" PC BOARDS</u>	<u>%/1000 HOURS FAILURE RATE</u>
13.2 W.	3.43	
12.8 W.	2.63	
2.6 W.	0.64	
19.2 W.	0.30	
9.5 W.	0.25	
1 W.	0.85	
24.6 W.	(220 IN ³ ASSY)	2.55
81.9 W.	9 PCB'S + POWER SUPPLY ASSEMBLY	10.65%/1000 HOURS

TABLE A-3
CONTROL UNIT POWER, SIZE, RELIABILITY

	<u>POWER</u>	<u>NO. OF 9" x 6.9" PC BOARDS</u>	<u>%/1000 HOURS FAILURE RATE</u>
DIGITAL FILTERS	21 W	2	2.63
TAPE RECORDER INTERFACE (48 TRACKS)	16 W	1	
DATA BUFFER MEMORY	4 W	3	
FORMATTER	16 W	2	
PARTY LINE INTERFACE	9.5 W	1	
POWER SUPPLY (70% EFF.)	28.5 W	(220 IN ³ ASSY)	2.55
	95 W	9 PCB'S + POWER SUPPLY ASSEMBLY	15.48

TABLE A-4
ESTIMATED WEIGHT BREAKDOWN - REMOTE UNIT

<u>ITEM</u>	<u>WEIGHT-LBS</u>
HOUSING	4.90
ACCESS COVER	.34
MOTHER BOARD ASSEMBLY	.75
I/O CONNECTORS	.75
PW BOARD ASSEMBLYS (X9)	7.49
CONFORMAL COATING	.11
WIRING	.23
POWER SUPPLY	9.24
GASKETING	.10
MISCELLANEOUS SCREWS AND HARDWARE	.10
TOTAL	24.01

TABLE A-5
ESTIMATED WEIGHT BREAKDOWN - CONTROL UNIT

<u>ITEM</u>	<u>WEIGHT-LBS</u>
HOUSING	4.90
ACCESS COVER	.34
MOTHER BOARD ASSEMBLY	.75
I/O CONNECTORS	.70
PW BOARDS ASSEMBLYS (X9)	7.49
CONFORMAL COATING	.11
WIRING	.21
POWER SUPPLY	8.64
GASKETING	.10
MISCELLANEOUS SCREWS AND HARDWARE	.10
TOTAL	23.34

TABLE A-6
RELIABILITY ESTIMATE
AIRBORNE ENCODER/FORMATTER SYSTEM

BASIS: MIL-HDBK-217C, PARTS COUNT METHOD

ASSUMPTIONS:

- ° A_{IT} ENVIRONMENT (AIRBORNE INHABITED TRANSPORT)
- ° AMBIENT TEMPERATURE 57.2°C (135°F)
- ° PACKAGE DESIGN (REMOTE UNIT AND CONTROL UNIT) WITH 9.75" W x 8.38" H x 8.25" L ALUMINUM HOUSING (SIZE INCLUDES .5" COOLING FINS SPACED APPROXIMATELY .45" APART)
- ° PARTS QUALITY:

INTEGRATED CIRCUITS - CLASS B

DISCRETE SEMICONDUCTORS - JANTX

RESISTORS AND CAPACITORS - FAILURE RATE LEVEL P

RELIABILITY CALCULATION FOR A 144 CHANNEL SYSTEM (9 REMOTE UNITS + 1 CONTROL UNIT):

TOTAL FAILURE RATE =

$9 \times 10.65 + 15.48 = 111.33\% / 1000 \text{ HOURS}$ WHICH IS EQUIVALENT TO
898 HOURS MTBF

TABLE A-7
AIRBORNE POWER, WEIGHT, SIZE SUMMARY
(144 CHANNEL PCM SYSTEM)

<u>ITEM</u>	<u>QUANTITY</u>	<u>POWER (WATTS) EACH</u>	<u>WEIGHT (LBS) EACH</u>	<u>SIZE (FT³) EACH</u>
REMOTE UNITS	9	81.9	24.01	0.437
CONTROL UNIT	1	95	23.34	0.437
*TAPE TRANSPORTS	2	150	49	1.11
RECORD ELECTRONICS ASSEMBLIES	4	60	10	0.31
TOTAL		1372 WATTS	377 LBS	7.83 FT ³

* INCLUDING TAPE AND SHOCK MOUNTS

$$\text{MODULARITY} = \frac{\text{TOTAL SYSTEM VOLUME}}{\text{VOLUME OF LARGEST COMPONENT}} = \frac{7.83}{1.11} = 7.05$$

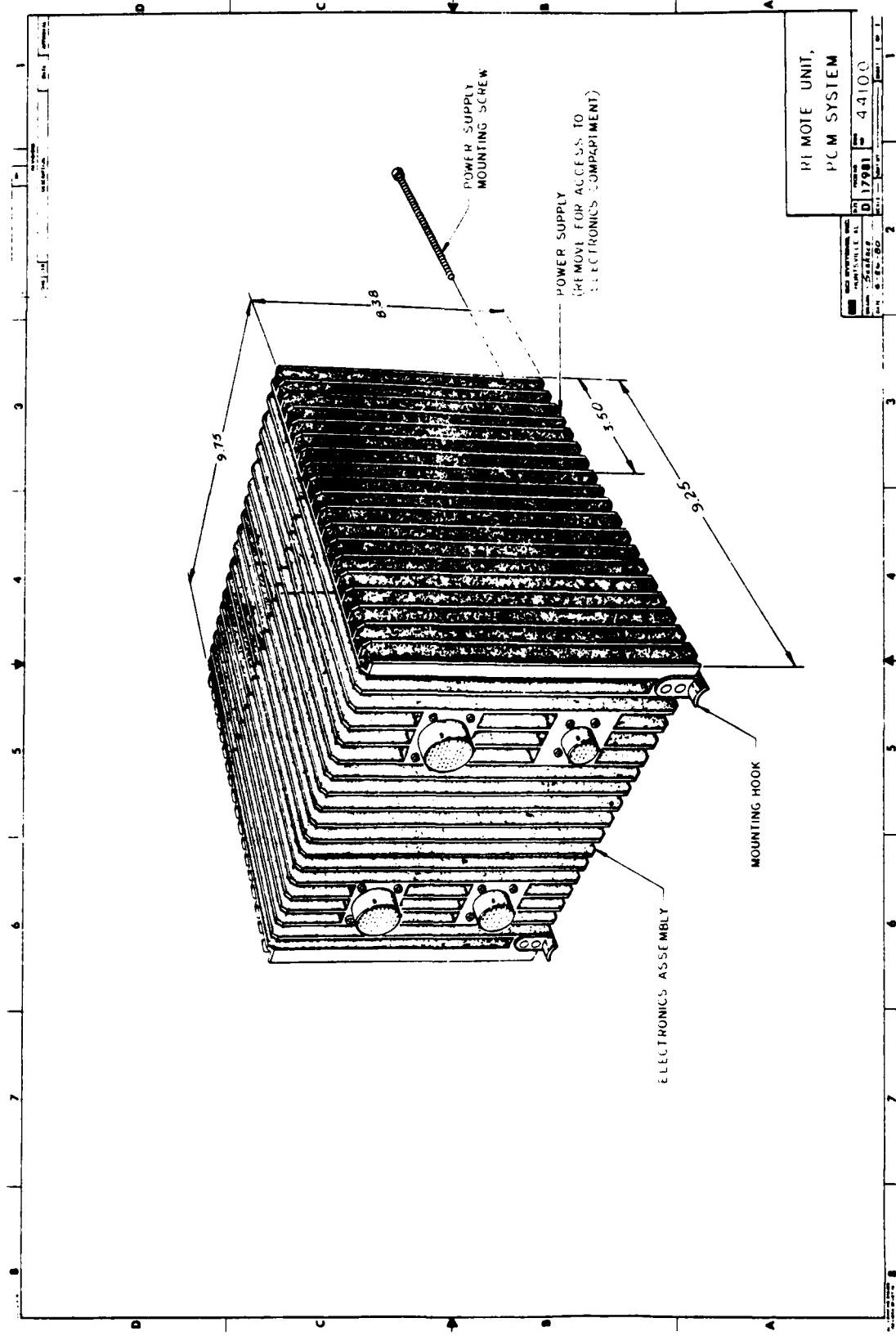


FIGURE A-1

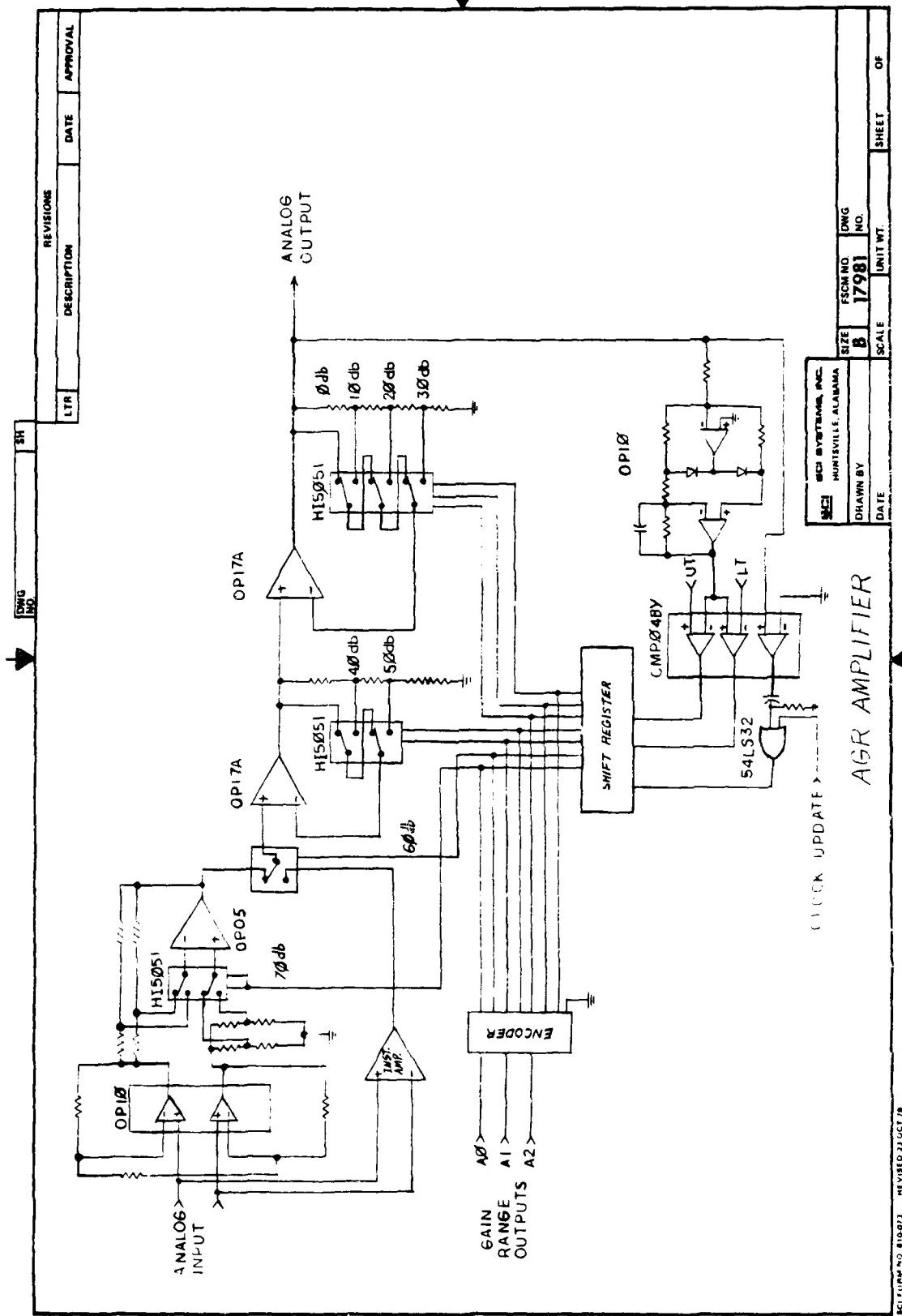


FIGURE A-2
AUTOMATIC GAIN RANGING AMPLIFIER

AD-A104 775

MCDONNELL AIRCRAFT CO ST LOUIS MO

F/G 14/2

APPLICATION OF PULSE CODE MODULATION (PCM) TECHNOLOGY TO AIRCRAFT--ETC(U)

APR 81 C A DETMER, C J GUNTHER, J H RIXLEBEN F33615-79-C-3205

AFWAL-TR-81-3017

NL

UNCLASSIFIED

2 of 5

60
NOV 1981

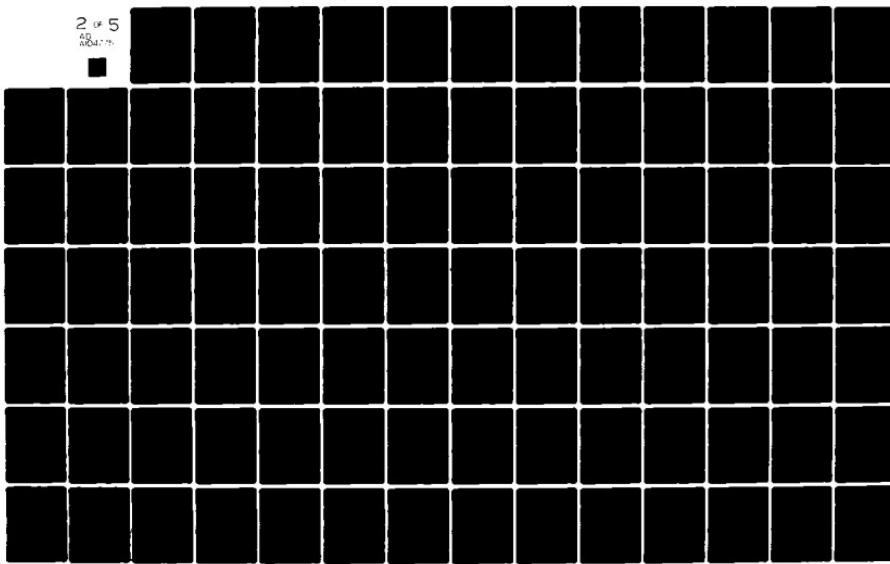


TABLE A-8
ANALOG LOW PASS FILTERS
(4 PER DATA CHANNEL)

CIRCUIT CONFIGURATION: ACTIVE VCVS AS SHOWN ON PAGE 80.

CUTOFF FREQUENCIES: 20 KHZ, 5 KHZ, 1250 HZ, 312.5 HZ

CHARACTERISTICS: TYPE I CHEBYSHEV WITH 0.1 DB (PEAK TO PEAK) PASSBAND RIPPLE. THIS CORRESPONDS TO THE FOLLOWING NORMALIZED POLE LOCATIONS IN THE COMPLEX PLANE:

$$\begin{aligned} & -0.083840966 \pm j1.041833334 \\ & -0.234917165 \pm j0.835485465 \\ & -0.339465139 \pm j0.463659453 \\ & -0.376777879 \end{aligned}$$

EFFECTS OF PASSIVE COMPONENT TOLERANCES: 1% INITIAL TOLERANCES IN ALL RESISTORS AND CAPACITORS WILL RESULT IN GAIN AND INTER-CHANNEL PHASE ERRORS AS FOLLOWS AT CUTOFF:

	<u>NOMINAL</u>	<u>LOW</u>	<u>HIGH</u>
GAIN RESPONSE	-.1 DB	-1.08 DB	+0.83 DB
INTER-CHANNEL PHASE DIFFERENCE BETWEEN FILTERS OF LIKE CUTOFF FREQUENCY	0°	-8.17°	+8.17°

BY TRIMMING THE FILTERS DURING MANUFACTURE THE INITIAL INTER-CHANNEL PHASE ERROR CAN BE ELIMINATED.

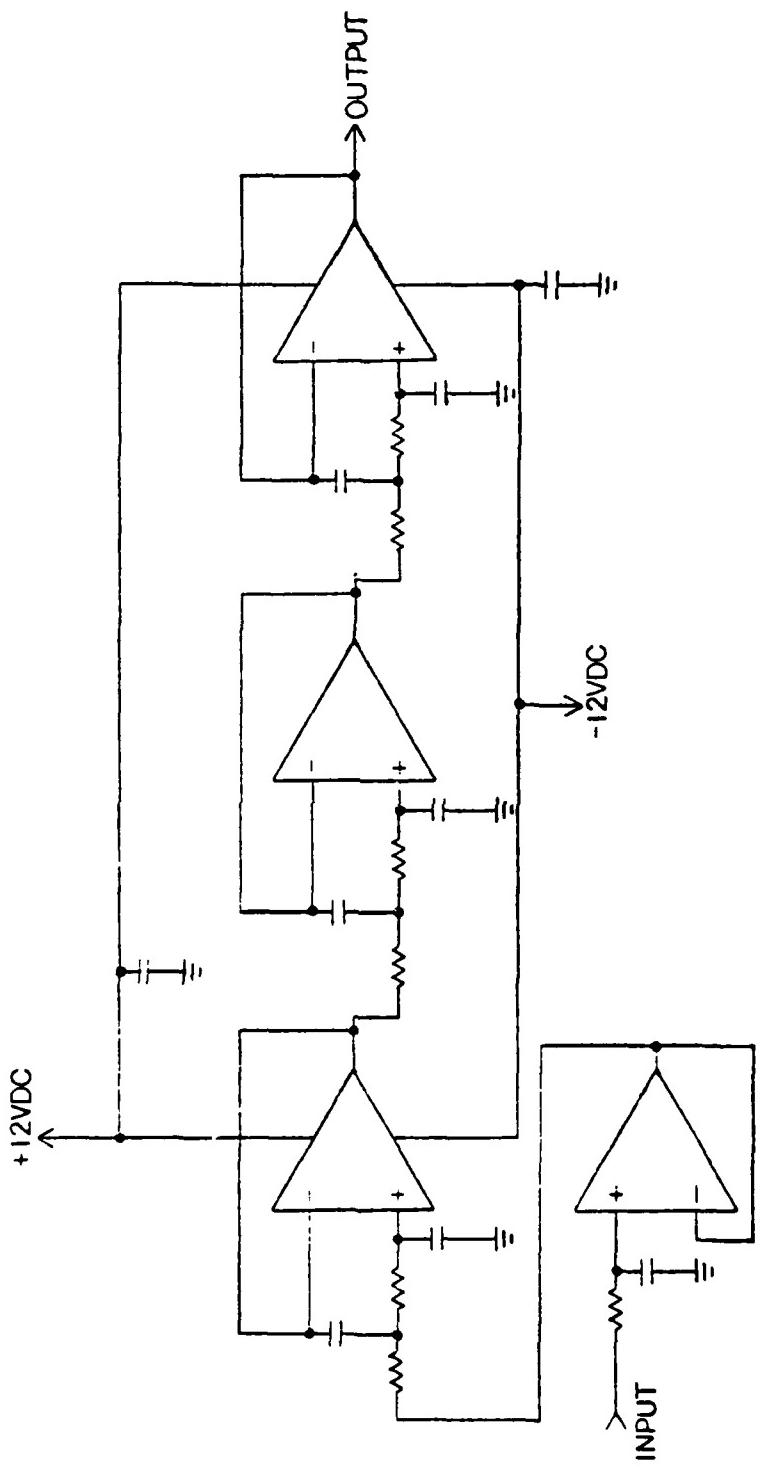


FIGURE A-3
7-POLE CHEBYSHEV LOWPASS VCVS FILTER

TABLE A-9
 AIRBORNE SYSTEM
 NON-RECURRING COST SUMMARY (LESS AGR AMPLIFIER)
 PROVIDED BY SCI SYSTEMS, INCORPORATED

1.0 DESIGN, DEVELOPMENT, TEST AND EVALUATION	<u>\$K</u>
1.1 DESIGN ANALYSES	120.0
1.1.1 Remote Unit	30.0
1.1.1.1 Filters	12.0
1.1.1.2 ADC	5.0
1.1.1.3 Control Logic	5.0
1.1.1.4 Power Supply	3.0
1.1.1.5 Mechanical Design	5.0
1.1.2 Control Unit	65.0
1.1.2.1 Data Channel Interface	9.0
1.1.2.2 Digital Filter	12.0
1.1.2.3 Data Buffer Memory	10.0
1.1.2.4 Format Controller	16.0
1.1.2.5 Tape Recorder Interface	10.0
1.1.2.6 Power Supply	3.0
1.1.2.7 Mechanical Design	5.0
1.1.3 Development Data	15.0
1.1.3.1 Development Test Plan	2.0
1.1.3.2 Software Dev. Plan	2.0
1.1.3.3 Prelim System Spec	3.0
1.1.3.4 Thermal Analysis	4.0
1.1.3.5 Reliability Analysis	4.0
1.1.4 Concept Design Review	10.0
1.2 BREADBOARD DEVELOPMENT	105.0
1.2.1 Remote Unit	27.0
1.2.1.1 Filters	15.0
1.2.1.2 ADC	5.0
1.2.1.3 Control Logic	4.0
1.2.1.4 Power Supply	3.0

1.2.2 Control Unit	60.0
1.2.2.1 Data Channel Interface	9.0
1.2.2.2 Digital Filter	12.0
1.2.2.3 Data Buffer Memory	10.0
1.2.2.4 Format Controller	18.0
1.2.2.5 Tape Recorder Interface	8.0
1.2.2.6 Power Supply	3.0
1.2.3 Data	8.0
1.2.3.1 Schematics	3.0
1.2.3.2 Parts Program Plan	1.0
1.2.3.3 Outline Drawings	2.0
1.2.3.4 Weight Analysis	2.0
1.2.4 Preliminary Design Review	10.0
1.3 PROTOTYPE DEVELOPMENT AND TESTING	204.0
1.3.1 Remote Unit (2 Ea)	60.0
1.3.1.1 System Engineering	10.0
1.3.1.2 Fabrication (incl Matl's)	30.0
1.3.1.3 Test	20.0
1.3.2 Control Unit (1 Ea)	34.0
1.3.2.1 System Engineering	4.0
1.3.2.2 Fabrication (Incl Matl's)	20.0
1.3.2.3 Test	10.0
1.3.3 System Integration and Test	60.0
1.3.4 Documentation	40.0
1.3.4.1 Prod Documentation	25.0
1.3.4.2 Acceptance Test Proc.	2.0
1.3.4.3 Development Test Report	3.0
1.3.4.4 Sys/Subsystem Spec	4.0
1.3.4.5 Programming Manual	6.0
1.3.6 Critical Design Review	10.0
1.4 QUALIFICATION UNIT DEVELOPMENT AND TEST	204.0
1.4.1 Remote Unit (2 Ea)	60.0
1.4.1.1 System Engineering	10.0
1.4.1.2 Fabrication	30.0
1.4.1.3 Test	20.0

1.4.2 Control Unit		34.0
1.4.2.1 System Engineering	4.0	
1.4.2.2 Fabrication	20.0	
1.4.2.3 Test	10.0	
1.4.3 System Integration and Test		85.0
1.4.4 Data and Documentation		15.0
1.4.4.1 Qualification Test Proc.	2.0	
1.4.4.2 Qualification Test Report	3.0	
1.4.4.3 Documentation Clean-Up	10.0	
1.4.5 Final Design Review		10.0
1.5 TEST EQUIPMENT		155.0
1.5.1 Integrated Test Set		100.0
1.5.1.1 Design and Software Dev.	35.0	
1.5.1.2 Fab./Procurement (1 Ea)	50.0	
1.5.1.3 Verification Testing	15.0	
1.5.2 EPROM Programmer		25.0
1.5.2.1 Design and Software Dev.	5.0	
1.5.2.2 Fab./Procurement (1 Ea)	15.0	
1.5.2.3 Verification Testing	5.0	
1.5.3 Quick-Look Pre-Flight Test Set		30.0
1.5.3.1 Design and Software Dev.	2.0	
1.5.3.2 Fab./Procurement (1 Ea)	25.0	
1.5.3.3 Verification Testing	3.0	
1.6 SYSTEM ENGINEERING AND MANAGEMENT		80.0
TOTAL DDT&E		\$868.0 K

TABLE A-10
AIRBORNE SYSTEM
RECURRING COST SUMMARY

PCM ENCODER/FORMATTER SYSTEM (COST ESTIMATES BY SCI SYSTEMS, INCORPORATED BASED ON PURCHASE OF TWO [2] 144 CHANNEL SYSTEMS)

<u>QTY</u>	<u>DESCRIPTION</u>	<u>COST EACH</u>	<u>TOTAL</u>
1	CONTROL UNIT	\$ 30,000	\$ 30,000
9	REMOTE UNITS	26,100	234,900
	SUPPORT EQUIPMENT	59,000	59,000
TOTAL			\$323,900

TAPE RECORDERS (COST QUOTATIONS FROM SANGAMO BASED ON PURCHASE OF FIVE [5] RECORDERS)

<u>QTY</u>	<u>DESCRIPTION</u>	<u>COST EACH</u>	<u>TOTAL</u>
2	28 TRACK RECORDERS	\$ 53,985	\$107,970
2	FLIGHT CONTROL UNITS	1,110	2,220
1	GROUND CONTROL UNIT	2,250	2,250
1	OSCILLOSCOPE DISPLAY	1,990	1,990
2	DIRECT REPRO. AMPS.	310	620
14	DIRECT EQUALIZERS	70	980
TOTAL			\$116,030

TOTAL RECURRING COST FOR A 144 CHANNEL AIRBORNE SYSTEM \$439,930

TABLE A-11a
 GROUND ANALYSIS SYSTEM THROUGHPUT
 (HOST COMPUTER AND ARRAY PROCESSOR)

	HOST COMPUTER		
AVERAGE OF 31 CANDIDATES	RAYTHEON 704	DEC VAX 11/780	
.209	.0294	.30	
4.79	.25	8.0	
2.31	2.0	5.5	
11.07	2.0	13.3	
575.6	5.0	1024	
CALCULATED HOST PERFORMANCE	5.0	1.248	8.47

* MILLION OPERATIONS PER SECOND

MEMORY INDEX (UNITY = 256 KB)

ARRAY PROCESSOR BUS INTERFACE RATE (MB/SEC)

HOST BUS RATE (MB/SEC)

DISK CAPACITY (MB)

* AS MEASURED BY FDC BENCHMARK PROGRAM

TABLE A-11b
ARRAY PROCESSOR PERFORMANCE

	ARRAY PROCESSOR		
AVERAGE OF 8 CANDIDATES	RAYTHEON 704	DEC VAX 11/780	
MEMORY INDEX (UNITY = 256 KB)			
TIME TO DO 1024 PT REAL FFT (MSEC)	4.35	40.8	2.7
TIME TO DO 1024 PT COMPLEX FFT (MSEC)	7.69	66.3	4.8
TIME TO DO 32 x 1024 PT CONVOLUTION (NSEC)	20.28	126	6.6
TIME TO DO 1024 PT COMPLEX MULTIPLY (MSEC)	1.50	8.5	0.52
CALCULATED ARRAY PROCESSOR PERFORMANCE	8.0	1.443	16.23

TABLE A-11C
SYSTEM PERFORMANCE = HOST PERFORMANCE + 1/5 ARRAY PROCESSOR PERFORMANCE

	HOST/ARRAY PROCESSOR SYSTEM	
AVERAGE SYSTEM	RAYTHEON SYSTEM	DEC/FPS SYSTEM
6.6	1.54	11.72

$$\frac{\text{DEC/FPS SYSTEM PERFORMANCE}}{\text{RAYTHEON SYSTEM PERFORMANCE}} = \frac{11.72}{1.54} = 7.61$$

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12. Rabiner, L. R. and Gold, B., Theory and Application of Digital Signal Processing, Prentice-Hall, 1975.

APPENDIX B

PHASE I INTERIM REPORT
APPLICATION OF PULSE CODE MODULATION (PCM)
TECHNOLOGY TO AIRCRAFT DYNAMICS DATA ACQUISITION

Revision date

Revision letter

Issue date 15 July 1979

Contract number F33615-79-C-3205

Prepared by

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Approved by

Carl Detmer

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INDEX OF PAGE CHANGES

REVISION DATE AND LETTER	PAGES AFFECTED			REMARKS	REVISED BY	APPROVED
	REVISED	ADDED	REMOVED			

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1. INTRODUCTION

This interim report is being submitted in compliance with Contract Data Requirements List (CDRL) Sequence Number 3 of Attachment Number 1 to Contract F33615-79-C-3205. It covers the contractor's (McDonnell Aircraft Company) work on Phase I (Facility Review, Literature Search, Formulation of System Standards and System Goals) of the study authorized by this contract.

1.1 OVERALL STUDY OBJECTIVES

The objectives of this study are to provide AFWAL/FIBG with the following:

- (a) The design of an optimum Pulse Code Modulation (PCM) data acquisition, playback, and analysis system utilizing all, part, or none of the present facility equipment, and
- (b) knowledge of the rationale, considerations, and judgements involved in the creation of that design.

The study involves four phases of effort as follows:

Phase I - Facility Review, Literature Search, Formulation of System Standards and System Goals

Phase II - Definition of PCM Systems

Phase III - Evaluation of PCM Systems

Phase IV - PCM System Design

The results of each phase must be approved by AFWAL/FIBG prior to starting work on the next phase.

1.2 PHASE I OBJECTIVES

The objectives of Phase I of the study are as follows:

- (a) To formulate system standards to be used in evaluating PCM data acquisition, analysis, and display processes.
- (b) To evaluate AFWAL/FIBG's existing facility according to the system standards.

(c) To develop a set of performance goals for the design of a new PCM system.

(d) To conduct a literature search of the existing sources of scientific and technical information to determine the current state-of-the-art in PCM technology.

1.3 SCOPE OF PHASE I EFFORT

The primary thrust of the study is toward a PCM system for airborne data acquisition (and subsequent analysis and display), although AFWAL/FIBG has capabilities and requirements for ground testing using its mobile vans. The standards and goals and facility evaluation data provided apply to the airborne application.

2. PHASE I RESULTS

2.1 SYSTEM STANDARDS

The system standards are measures by which the alternate PCM systems determined in Phase II of this study can be compared with each other and with the capabilities of AFWAL/FIBG's existing equipment. Thus, the standards consist of performance criteria and characteristics that are of concern to the user of the system. As a result of Phase I, MCAIR has determined the standards to be as listed and defined in Sections 2.1.1 through 2.1.3. These were obtained by considering both AFWAL/FIBG's test operational requirements and the types of analysis that are generated from the test data. The AFWAL/FIBG data system has been divided into three categories and standards established for each - Data Acquisition, Analysis and Display (Figure B-1).

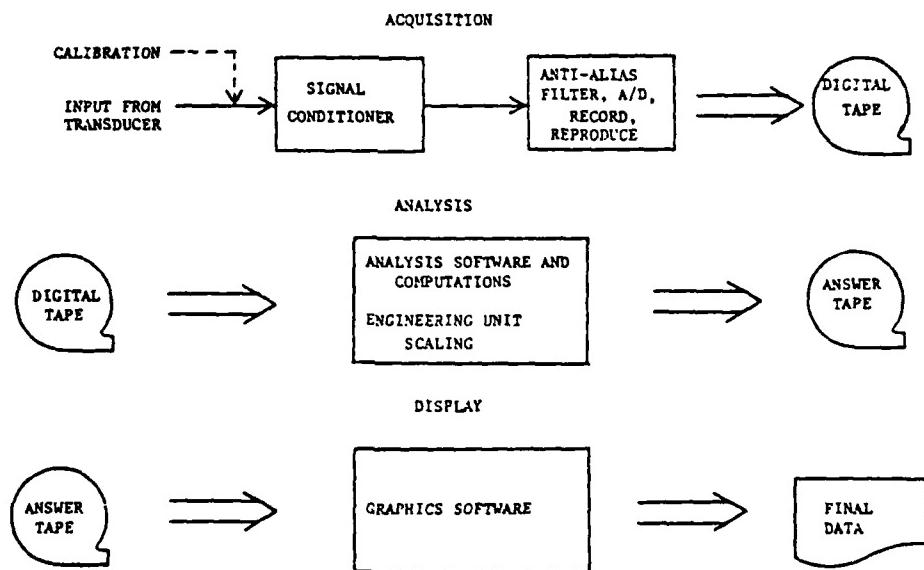


FIGURE B-1 - DEFINITIONS

Data acquisition includes all components and processes from the signal conditioner input terminals to the digital data-storage medium for entry to the analysis system. Analysis includes all components and processes from the digital data entry through the generation of the scaled answers. Display includes the software and the printer/plotter used to generate the final data outputs.

2.1.1 DATA ACQUISITION STANDARDS

(a) Measurand Channel Bandwidth - This is defined to be the continuous frequency interval where the amplitude response is flat within ± 1 dB, referenced to the response at zero Hertz. Bandwidth is exclusive of transducer, but does include all signal conditioning and the encoder. This is a large signal bandwidth (i.e., no slew rate limiting at the highest frequency for a full-scale signal at the encoder). Bandwidth applies under environmental conditions.

(b) Accuracy - Accuracy is the ratio of the error (measured at DC and referred to the encoder input) to the full-scale encoder expressed in %. It includes all signal conditioning and the encoder, calculated as the root-sum-of-squares of individual component errors under environmental conditions.

(c) Encoding Resolution - This is the number of bits (including sign bit) used to encode the signal. Any bits used to represent gain status for systems employing auto-ranging will be considered separately.

(d) Dynamic Range - Dynamic Range is defined as:

$$\text{Dynamic Range} = 20 \log_{10} \frac{\text{Espan}}{N_{\text{RMS}}} \quad (1)$$

where: Espan is the input voltage span of the acquisition system (at a fixed gain setting), and N_{RMS} is the total RMS noise for all signal conditioning and the encoder, measured over the entire measurand channel bandwidth, under environmental conditions, and referred to the input. Additional contributions

to dynamic range by auto-range capability will be considered separately.

(e) Number of Measurands Acquired Simultaneously - This is the number of individual transducer signals that can be recorded together during a given test, exclusive of voice annotation and time code.

(f) Inter-Channel Phase Error - Inter-channel phase error is the phase difference between any two measurand channels measured at 10 kHz, exclusive of linear phase shifts caused by known fixed time delays that are corrected in the analysis.

(g) Total Record Time Capability - This is the total length of time that can be recorded for an airborne test, utilizing all available measurand channels at their maximum frequency response capability.

(h) Airborne Volume - This is the space occupied by all airborne data acquisition components, including mounting structure and inter-module cabling, but excluding transducers and input signal cabling.

(i) Airborne Weight - This is the weight of all airborne data acquisition components including mounting structure and inter-module cabling, but excluding transducers and input signal cabling.

(j) Degree of Modularity - This is defined as the ratio of the airborne volume to the volume of the largest component of the airborne acquisition system.

(k) Environmental Conditions - Applicable environmental conditions are temperature, altitude, shock and vibration, humidity, sand and dust.

(l) Power Requirements - This is defined as the number of watts required by all airborne data acquisition equipment.

(m) Reliability - This is an estimate of the mean time between failures in the airborne data acquisition equipment.

(n) Maintainability - This is an estimate of the mean time to repair the airborne data acquisition system.

(o) Test Readiness - Test readiness is a measure of the time required to configure, install, calibrate and check out the airborne data acquisition system for a particular test mission.

(p) Capability for On-Site Data Evaluation - This consists of sufficient ground support equipment to be used for quickly and accurately evaluating data recordings in the field, immediately after a test mission.

(q) Operational Flexibility - This includes the choice of sample rates, bandwidths, record times, and number of channels in the data acquisition system, and the skill level required of the operator.

(r) Recurring Manpower Support - This is the number of people AFWAL/FIBG needs to send to the field for installation, calibration, and maintenance of the airborne data acquisition system.

(s) System Hardware Cost - This is the cost of one set of equipment required for the airborne portion of the data acquisition system. It excludes non-recurring expenses.

2.1.2 ANALYSIS STANDARDS

(a) Maximum Array Size - This is the largest number of data samples that can be processed in memory by one array operation.

(b) Choice of Analysis Types - This is a measure of the capability of the data analysis system to perform specific types of data analysis. It is recognized that this standard will influence the data acquisition system also, since the method of acquiring data must not preclude the possibility of analyzing it in the required manner.

(c) Statistical Accuracy - Analyses of random data are subject to statistical errors (bias and variance). These errors manifest themselves as

distortions of spectral peaks and valleys (bias error) and random scatter about the true value (variance error). The bias error is highly data dependent and is generally small for analyses with good frequency resolution. The variance error is usually of more concern. It is a function of the product of the analysis bandwidth (B) and the data record length (T). The variance error diminishes as the BT product is increased. For analyses performed using the fast Fourier transform and a rectangular data window with no overlap, the BT product is simply equal to the number of transforms averaged. The amount of variance error is dependent on the type of analysis as well as the BT product. Therefore, the BT product will be used as the standard to indicate statistical accuracy, independent of the type of analysis.

- (d) Computer Precision - This is the number of bits and word format used by the computer in performing the analysis computations.
- (e) Edit Capability - Edit capability is the number of measurand channels that can be displayed per pass through the original data for editing purposes.
- (f) Throughput - This is the number of analyses that can be performed per unit time.
- (g) Recurring Manpower - The number of manhours per unit time required to maintain and operate the data analysis facility.
- (h) System Hardware Cost - This is the total cost of the ground data analysis system. (For the present Flight Dynamics Laboratory facility, this will include some components that are functionally acquisition oriented, e.g., A/D conversion system, anti-alias filters, etc.)
- (i) System Installation and Checkout Cost - This is the cost to install and make operational the data analysis system.
- (j) Software Development Cost - This is the cost to develop and make operational the software necessary to produce the required analyses, including

engineering units scaling.

2.1.3 DISPLAY STANDARDS

- (a) Throughput - This is the number of 8-1/2 X 11 inch plot pages that can be produced per unit time.
- (b) Resolution - This is the plot resolution in dots per unit length.
- (c) Choice of Formats - This is a measure of the types of symbols and characters that can be generated on a plot page.
- (d) Recurring Manpower - This is the number of manhours per unit time required to maintain and operate the data display facility.
- (e) System Hardware Cost - This is the total hardware cost of the display system.
- (f) System Installation and Checkout Cost - This is the cost to install and make operational the display system.
- (g) Software Development Cost - This is the cost to develop and make operational software necessary to generate final data analysis plots and tabulations.

2.2 FACILITY EVALUATION

Information regarding overall capabilities was obtained in conjunction with the contract "Kickoff Meeting" on 1 May 1979. Detailed information corresponding to the agreed upon system standards was obtained from AFWAL/FIBG by Messrs. Carl Detmer and Chuck Guenther of MCAIR and Don Ellis of SCI Systems, Inc. during the facility review trip 30 May - 1 June 1979.

2.2.1 GENERAL CAPABILITIES - The following is a summary of test capabilities and operational features of the AFWAL/FIBG test facility.

The facility is maintained to provide unique capabilities in testing and analysis of structural dynamics (vibration and aeroelasticity) in aircraft, missiles and space vehicles. The operation consists of a Dynamics Test Group

for instrumentation and data acquisition, a Data Analysis Group for processing and analysis of the data and a Project Engineering Group for test planning and test technology. The organization consists of 32 people.

The Dynamics Test Group provides instrumentation and expertise for acquisition of a broad spectrum of dynamics data from both flight and ground tests. Their equipment includes flight data acquisition packages and two mobile data acquisition and analysis vans that can be used at remote sites.

The Data Analysis Group provides processing and analysis of all types of analog and digital data. The data entry medium is magnetic tape. Most of the data collected by the Test Group is in analog form recorded on a 14-track tape recorder. Low frequency data up to 43 channels can be sampled using pulse-amplitude modulation (PAM) and recorded on one track. Voice annotation can be recorded on edge tracks or data tracks.

The number of dynamics data channels in the airborne system is limited to 12 at any one time. Selection of additional channels is accomplished by a stepper switch in the input cable junction box. The mobile van contains the facility for land lines, amplifiers and tape recorders to accommodate up to 36 dynamics data channels for acquisition and limited analysis.

The Data Analysis operation consists of:

- (1) Data recovery and editing
- (2) Analog-to-digital conversion
- (3) Digital analysis and
- (4) Graphic data representation.

The data is played back from the acquisition tape and edited for bad data, and a 1/3-octave band analysis is performed. The significant data segments are selected, digitized and recorded to provide a compatible input for digital computer processing. Time and frequency domain analyses, such

as correlation, power spectral density and transfer functions, are performed in the digital computer facility. The results of data analysis are plotted and presented in graph form in accordance with the user's requirements.

2.2.2 BASELINE EVALUATION PER STANDARDS - The evaluation of AFWAL/FIBG's facility per the system standards establishes current capabilities for data acquisition, analysis and display. The baseline configuration is as shown in Figures B-2 through B-4.

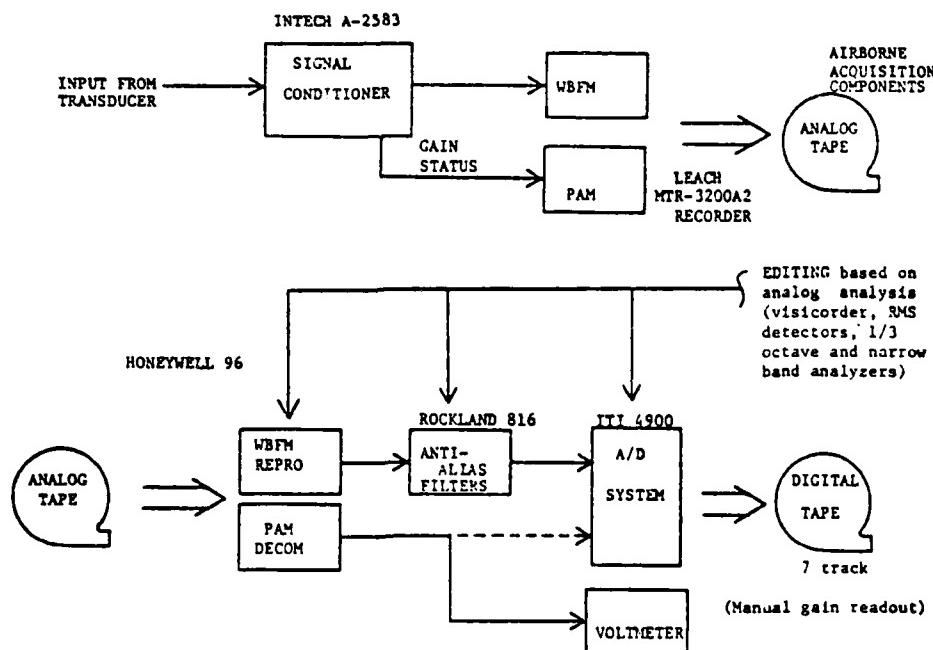


FIGURE B-2 - AFWAL/FIBG ACQUISITION BASELINE

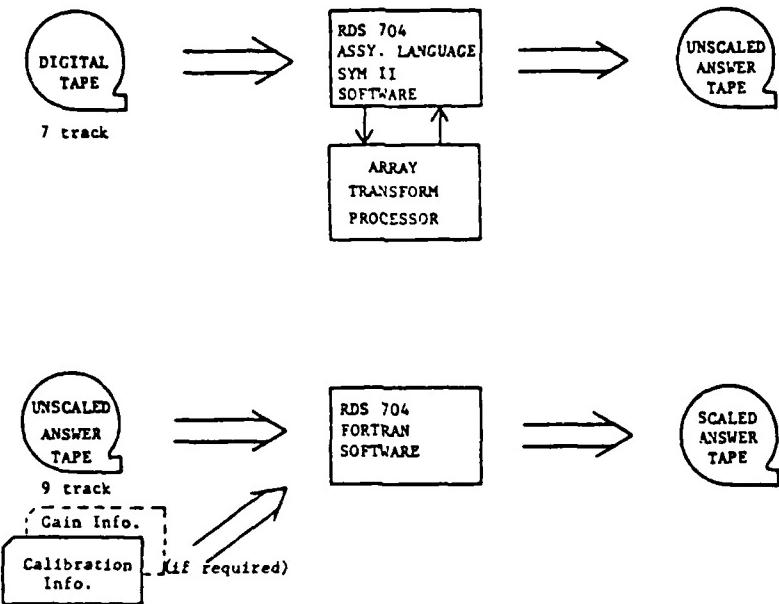


FIGURE B-3 - AFWAL/FIBG ANALYSIS BASELINE

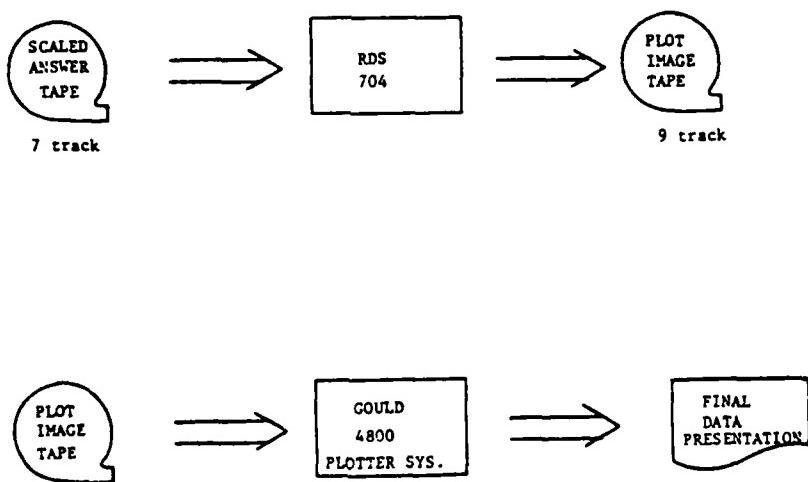


FIGURE B-4 - AFWAL/FIBG DISPLAY BASELINE

The results of the evaluation of the baseline system are indicated with the corresponding standards in Tables B-1 through B-3, except as expanded upon below. These results were, in most cases, obtained directly from AFWAL/FIBG

(a) Operational Flexibility (Acquisition) - Operational flexibility is provided in the current AFWAL/FIBG facility by the following:

- (1) Choice of tape speeds to trade bandwidth for recording time.
- (2) A programmable anti-alias filter (60 discrete filter cutoff frequency choices).
- (3) A selection of 14 discrete sample rates ranging from 130 Hz to 30 kHz.

(b) Throughput (Analysis) - The 40 transfer functions per hour is based on 16 averages of 4096-point transforms.

TABLE B-1
ACQUISITION PROCESS

<u>ACQUISITION STANDARDS</u>	<u>FIBG PRESENT CAPABILITY</u>	<u>GOAL FOR PCM SYSTEM</u>
MEASURAND CHANNEL BANDWIDTH	DC-20KHz	DC-20KHz
ACCURACY	.3-5%	.05%
ENCODING RESOLUTION	12 bits + 8 levels of autorange	12 bits + 8 levels of autorange
DYNAMIC RANGE	40-50DB + 70DB span of autorange	66DB + 70DB span of autorange
NO. OF MEASURANDS ACQUIRED SIMULTANEOUSLY	12	144
INTER-CHANNEL PHASE ERROR	5°	5°
TOTAL RECORD TIME CAPABILITY	7.5 min	8 hrs.
AIRBORNE VOLUME	4 cu. ft.	2 cu. ft.
AIRBORNE WEIGHT	110 lb.	50 lb.
DEGREE OF MODULARITY	2.62	
ENVIRONMENTAL CONDITIONS	Airborne	MIL E 5400 Class 2
POWER REQUIREMENTS	112 watts @ 28VDC	112 watts @ 28VDC (MIL STD 704)
RELIABILITY	N.A.	1000 hrs. MTBF
MAINTAINABILITY	N.A.	
TEST READINESS	N.A.	
CAPABILITY FOR ON-SITE DATA EVALUATION	Sometimes	Always
OPERATIONAL FLEXIBILITY	(See text)	
RECURRING MANPOWER SUPPORT	2	
SYSTEM HARDWARE COST	\$75,295 (1978 dollars)	

N.A. = DATA NOT AVAILABLE FROM AFWAL/FIBG

TABLE B-2
ANALYSIS PROCESS

<u>ANALYSIS STANDARDS</u>	<u>FIBG PRESENT CAPABILITY</u>	<u>GOAL FOR PCM SYSTEM</u>
MAXIMUM ARRAY SIZE	8192 16 BIT WORDS	16384 16 BIT WORDS
CHOICE OF ANALYSIS TYPES		
AUTO PSD	YES	YES
CROSS PSD	YES	YES
AMPLITUDE SPECTRA	YES	YES
TRANSFER FUNCTION	YES	YES
COHERENCE	YES	YES
MODAL ANALYSIS	NO	YES
ZOOM TRANSFORM	NO	YES
1/3 OCTAVE ANALYSIS	YES	YES
RMS TIME HISTORY	YES	YES
AUTO-CORRELATION	YES	YES
CROSS-CORRELATION	YES	YES
PROBABILITY DENSITY	YES	YES
PEAK PROBABILITY DENSITY	YES	YES
STATISTICAL ACCURACY (BT PRODUCT)	16	64
COMPUTER PRECISION	16 BITS FIXED POINT	32 BITS FLOATING POINT
EDIT CAPABILITY	6 CHANNELS	12 CHANNELS
THROUGHPUT	40 TRANSFER FUNCTIONS PER HOUR, MAX. (SEE TEXT)	
RECURRING MANPOWER	2	
SYSTEM HARDWARE COST	\$951,394 (1978 DOLLARS)	
SYSTEM INSTALLATION AND CHECKOUT COST	\$88,000 (1978 DOLLARS)	
SOFTWARE DEVELOPMENT COST	N.A.	

N.A. = Data not available from AFDDL/FBG.

TABLE B-3
DISPLAY PROCESS

<u>DISPLAY STANDARDS</u>	<u>FIBG PRESENT CAPABILITY</u>	<u>GOAL FOR PCM SYSTEM</u>
THROUGHPUT	.5 8-1/2 X 11" PLOTS/SEC	.5 8-1/2 X 11" PLOTS/SEC
RESOLUTION (DOTS PER INCH)	80	160
CHOICE OF FORMATS	STANDARD CALCOMP	STANDARD CALCOMP
RECURRING MANPOWER	1	
SYSTEM HARDWARE COST	\$27,140 (1978 DOLLARS)	
SYSTEM INSTALLATION AND CHECKOUT COST	N.A.	
SOFTWARE DEVELOPMENT COST	N.A.	

N.A. = DATA NOT AVAILABLE FROM AFWAL/FBG

2.3 PCM SYSTEM GOALS

Goals for the PCM system were established in discussions with AFWAL/FIBG personnel during the facility review trip (May 30 - June 1, 1979). These goals are indicated in Tables B-1, B-2, and B-3 for acquisition, analysis, and display, respectively. Many of the goals exceed AFWAL/FIBG's current capability. In these cases, the goals are considered to be desirable objectives to strive for in the PCM system design. In most instances, the current capability represents a minimum performance level for the new system. However, there are a few standards for which a lower level of performance than now exists, might be judged acceptable in a PCM system meeting other goals. These are enumerated and discussed below.

(a) Measurand Channel Bandwidth - AFWAL/FIBG has indicated (in the Contract Statement of Work) that 10 kHz would be an acceptable bandwidth for a PCM system.

(b) Airborne Volume, Weight, and Power Requirements - PCM acquisition and recording systems approaching some of the other goals (especially with respect to number of measurands and total record time) may turn out to be larger, weigh more, and consume more power than AFWAL/FIBG's present system. In this case, a greater degree of modularity could alleviate the overall size and weight problem.

2.4 LITERATURE SEARCH

The purpose of the literature search activity in Phase I is to obtain the necessary background materials and references in preparation for the Phase II detailed study of PCM system components and processes.

2.4.1 SOURCES FOR LITERATURE SEARCH

(a) Computer Literature Searches - Abstracts were obtained utilizing the following computer services:

- o Redstone Scientific Information Center
- o Lockheed DIALOG
- o MCAIR PDR (Pertinent Data Request)
- o Defense Documentation Center
- o NASA Scientific and Technical Information Facility.

(b) Manual Literature Searches - Pertinent material was obtained using the following sources:

- o MCAIR Library and Catalog
- o International Telemetering Conference Proceedings, 1966-1978
- o Science Abstracts, 1975-1978
- o International Aerospace Abstracts, 1975-1978
- o IEEE Spectrum, Proceedings, Transactions
- o NASA STAR Abstracts
- o Trade Journals: Computer Design, EDN, Electronics, Electronic Products.

(c) Vendor Survey - A letter was mailed to 84 manufacturers and users of airborne telemetry equipment to determine if onboard processing equipment is available or in development for acquiring acoustic and vibration measurements using PCM. (A copy of the letter is included in Section 4.) Replies have been received from 21 companies. The following companies indicated an interest in such equipment:

- o Avco Systems Div., Wilmington, Massachusetts (User of onboard processing modules manufactured by Gulton)
- o Bunker-Ramo Corp., Electronic Systems Division, Westlake Village, California (Onboard processor in development)
- o Gulton, Data Systems Division, Albuquerque, New Mexico (Analog processors off-the-shelf; digital processor being developed)

- o Harris Electronic Systems Division, Melbourne, Florida
(Digital processor in early stages of development)
- o SCI Systems, Huntsville, Alabama (Digital processor in conceptual stage).

(d) PCM Data Acquisition Component Survey - A preliminary survey was made of available data acquisition components (A/D's and multiplexers). A listing of components that represent the state-of-the-art is included Section 4.

2.4.2 LITERATURE AVAILABLE - Hard copies and/or microfiches are on hand for study by personnel for approximately 225 bibliography items. Twenty-two of these have been selected as the most useful for beginning Phase II. Abstracts of these items are provided in Section 4.

2.4.3 DATA ACQUISITION METHODS - CONCLUSIONS - Based on the literature search, there are six techniques for acquiring dynamic data digitally. One of these is by continuous sampling (obtaining and recording a time series of equal interval samples taking care to avoid aliasing). The other techniques take samples in a similar manner, but also involve some form of processing so that a reduction in data can be achieved prior to recording. The five techniques involving onboard processing are briefly summarized below.

(a) Multiple-Filter Encoding - This involves sampling the data through several different filters in sequence. Advantages of this technique are its relative simplicity and the potential for considerable amount of data compression. A disadvantage is decreased statistical accuracy (for a given data record length) in proportional bandwidth analyses such as 1/3 octave.

References:

- (1) P. I. Richards, "Computing Reliable Power Spectra", IEEE Spectrum, January 1967, pp. 83-90
- (2) R. D. Kelly, L. D. Enochson, "Techniques and Errors in Measuring Cross-Correlation and Cross-Spectral Density Functions", Measurement Analysis Corporation Report No. MAC 511-01, February 1966.
 - (b) Onboard Fast Fourier Transform (FFT) and Averaging - This technique involves real-time computations of the FFT over short data segments and averaging the answers. Data compression would result from the averaging. No loss in statistical accuracy would result from this technique. Further averaging, if necessary, could be done during ground data processing operations. Constant bandwidth analyses would result from this technique. Proportional bandwidth analyses (e.g. one-third octave) could be constructed as well. Data preprocessing operations (necessary prior to application of the FFT) such as mean and trend removal and windowing could be complicated in an airborne setup.

Reference: R. K. Otnes and L. Enochson, Digital Time Series Analysis, Wiley, 1972.

- (c) Onboard Direct Computation of Correlation Functions - Using this technique, all required correlation functions would be computed directly onboard using digital or analog signal processing. Data compression would result because the number of correlation lag values recorded would be considerably fewer than the number of data sample points used to generate them. Power spectral densities would then be computed using the FFT during ground processing operations. No loss in statistical accuracy would result using this technique. Constant bandwidth analyses would result. A serious drawback is the complexity involved if many combinations of cross-correlation

functions are required:

Reference : D. Jones, "An On-Board Digital Correlator for Spacecraft VLF Radio Wave Studies", IEEE Trans. Geoscience Electronics, Vol. GE-12, No. 1, 9 (1974).

(d) Signal Averaging (Rotating Memory) - This technique achieves data compression by time-domain averaging of the sampled data. (Adjacent samples are not averaged - the data is segmented and corresponding sample points in each segment are averaged.) Phase information is preserved with this relatively simple technique. Fourier transformation and averaging of answers is performed during ground processing. The method is best suited for handling periodic data where the time averaging can be synchronized with a known signal.

References:

- (1) D. Jones, "Signal Pre-Processing On Spacecraft", Space Science Instrumentation 3 (1977) pp. 171-185
- (2) Hewlett-Packard Application Note 245-1, "Signal Averaging with the HP3582A Spectrum Analyzer"
- (3) C. R. Trimble, "What is Signal Averaging?", Hewlett-Packard Journal April 1968.

(e) Onboard Filtered Power Spectral Densities (PSD's) - With this technique, analog or digital filters are used to separate the signal components which are then squared and summed to form answers proportional to power spectral density. A great deal of data compression is possible using this technique. To date, applications have been limited to auto PSD's (no phase), and best resolution has been 1/3 octave.

References:

- (1) N. H. Endsley, K. H. Lee, and R. H. Maschoff, "A Data Acquisition System Featuring On-Board Processing", ITC Proceedings, Vol. 13, pp. 113-129, 1977

- (2) R. H. Myers, Jr. and R. E. Fries, "Acoustic/Vibration Environment Experiment", ISA Paper ISBN 87664-362-4, 1977
- (3) R. H. Maschoff, "On-Board High Frequency Data Processing", ITC Proceedings, Vol. 10, pp. 529-535, 1974.

The above techniques were evaluated by MCAIR for compatibility with the analysis types listed as goals in Table B-2. The results of the evaluation are given in Table B-4. The only technique versatile enough to accommodate all types of analysis for all types of data is the basic continuous sampling method. However, assuming stationary test data, acquisition using the multiple filter encoding method also permits all of the desired analysis types to be employed.

TABLE B-4

COMPATIBILITY OF ONBOARD PROCESSING WITH ANALYSIS REQUIREMENTS

<u>ANALYSIS TYPE</u>	<u>CONTINUOUS SAMPLING</u>	<u>MULTIPLE FILTER ENCODING</u>	<u>ONBOARD FFT AND AVERAGE</u>	<u>ONBOARD CORRELATION</u>	<u>ONBOARD 1/3 OCTAVE RMS</u>	<u>SIGNAL AVERAGING</u>
AUTO PSD	YES	YES	YES	YES	YES	YES
CROSS PSD	YES	YES	YES	YES	NO	YES
AMPLITUDE SPECTRA	YES	YES	YES	YES	NO	YES
TRANSFER FUNCTION	YES	YES	YES	YES	NO	YES
COHERENCE	YES	YES	YES	YES	NO	YES
MODAL ANALYSIS	YES	YES*	YES	YES	NO	NO
ZOOM TRANSFORM	YES	YES*	YES	NO	NO	NO
1/3 OCTAVE ANALYSIS	YES	YES	YES	YES	YES	NO
RMS TIME HISTORY	YES	YES	YES	YES	YES	YES
AUTO-CORRELATION	YES	YES	YES	YES	NO	YES
CROSS-CORRELATION	YES	YES	YES	YES	NO	YES
PROBABILITY DENSITY	YES	YES	NO	NO	NO	NO
PEAK PROBABILITY DENSITY	YES	YES	NO	NO	NO	NO

* Except for transient data.

3. RECOMMENDATIONS

3.1 GOALS - DATA ACQUISITION

Based upon Phase I, two of the goals established during the facility review appear to be extraordinarily ambitious, when considered along with other goals. These are the .05% goal for accuracy and the 8-hour goal for total record time capability. Even though goals are considered to be desirable objectives rather than firm requirements, MCAIR feels that these particular goals will create difficulties in evaluating the various Phase II PCM systems in Phase III. (Systems which fall far short of goals which are heavily weighted will tend to cluster together in the evaluation.)

3.1.1 ACCURACY - A more reasonable goal for accuracy (based on the literature search - PCM data acquisition component survey) is 0.5%, considering the effects of environment and the 20-KHz goal for bandwidth. MCAIR recommends that the accuracy goal be changed accordingly.

3.1.2 TOTAL RECORD TIME CAPABILITY - An eight-hour recording of 144 20-KHz channels continuously sampled with 12-bit resolution would result in the storage of at least 2.5×10^{12} bits of information. A single 4600-foot reel of tape with 28 tracks packed at 30,000 bits per inch could store 4.6×10^{10} bits, corresponding to a maximum of 8.9 minutes recording time. However, using a multiple filter encoding scheme, the storage requirements can be reduced to approximately 10^{10} bits and the 8-hour goal becomes reasonable. As discussed in Section 2.4.3, the multiple filter scheme is compatible with the goal for choice of analysis types if stationary data is assumed. Therefore, MCAIR recommends that the study proceed with two goals as follows for total record time capability:

8 hours (stationary data)
7.5 minutes (transient data)

3.2 DATA ACQUISITION METHOD - As noted in Section 2.4.3, only the continuous sampling and multiple filter encoding methods provide enough versatility to accommodate all of AFWAL/FIBG's present and anticipated types of dynamic data analysis. Therefore, MCAIR recommends that Phase II effort be directed toward alternate configurations of continuous sampling and multiple filter encoding PCM systems.

3.3 CONTINUATION OF STUDY - Based on the results of Phase I as presented herein, MCAIR recommends that Phase II of the study should be initiated.

4. SUPPLEMENTAL DATA

LITERATURE SEARCH MATERIAL

<u>Item</u>	<u>Reference (Text)</u>	<u>Page</u>
Vendor Survey Letter	2.4.1 (c)	116
PCM Data Acquisition Component Survey (Table B-5)	2.4.1 (d)	117
Selected Abstracts	2.4.2	118-139

10 May 1979

Gentlemen:

McDonnell Aircraft Company is considering the use of some form of onboard pre-processing for acquiring acoustic and vibration measurements using pulse code modulation (PCM). These measurements are made in connection with aircraft flight testing. The onboard pre-processing would reduce the bandwidth required for recording and/or telemetry, while at the same time preserving essential spectral characteristics of the signals.

If your company has already developed, or is in the process of developing flight qualified electronics for such an application, I'd like to hear from you. Please telephone or send product descriptions to me at the address below.

Please advise us prior to taking any action that would incur expense to McDonnell Aircraft Company.

Thank you,

Chuck Guenther

Chuck Guenther
Senior Engineer
Advanced Data Systems Group
Flight Test Data Systems
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(314) 232-3173

TABLE B-5
PCM DATA ACQUISITION COMPONENT SURVEY

A/D CONVERTERS

<u>Conversion Time (us)</u>	<u>Power Dis. (mw)</u>	<u>S&H</u>	<u>Int Ref</u>	<u>Par Out</u>	<u>Ser Out</u>	<u>Device</u>	<u>Source</u>	<u>Price</u>
1.	2	2700				ADM-8316-12*	DDC	
2.	5	1400		X	X	MN5240-12*	Micro-net	
3.	8	2000		X	X	ADCN212BMM	Datel	\$215.00
4.	8	2150	X	X	X	ADCNS12BMM	Datel	259.00
5.	10	1800		X	X	ADC85-12*	Burr-Brown	
6.	13	745			X	MN5213H	Micro-net	
7.	13	915		X	X	MN5216H	Micro-net	
8.	20	2000		X	X	ADC-HX12BMM	Datel	169.00
9.	25	925		X	X	AD572S	AD	

- NOTES:
1. All are 12 Bits Resolution
 2. All are $\pm 1/2$ LSB Linearity.
 3. All are Hybrid Technology.
 4. All are MIL Temp Range except *.

MULTIPLEXERS

<u>Channels</u>	<u>Type</u>	<u>On Resis</u>	<u>Range</u>	<u>Device</u>	<u>Source</u>
4 (Diff)	CMOS	400	± 15	M11828A-2	Harris
4 (Diff)	CMOS	1500	± 1	M1509A-2	Harris
4 (Diff)	CMOS	1500	± 15	MKD409M	Datel
4 (Diff)	JFET	350	-15 to 12	LFL1509	National
8	CMOS	400	± 15	M11818A-2	Harris
8	CMOS	1500	± 15	MK-800M	Datel
8	CMOS	1500	± 15	M1508A-2	Harris
8	JFET	350	-15 to 12	LFL1508	National
8 (Diff)	CMOS	270	± 15	MVD-807M	Datel
8 (Diff)	CMOS	400	± 15	M1507-2	Harris
8 (Diff)	CMOS	1500	± 15	MKD-807M	Datel
8 (Diff)	CMOS	1500	± 15	M1507A-2	Harris
16	CMOS	400	± 15	M1506-2	Harris
16	CMOS	1000	-5 to 15	M11840	Harris
16	CMOS	1500	± 15	MK-1600M	Datel
16	CMOS	1500	± 15	M1506A-2	Harris
16	PMOS	5K	-5 to 15	M11840-2	Harris
32 w/ Memory	CMOS	50	± 9	MT88048	Mitel

DATA ITEM NO. 1

ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: PCM Technology Trends

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Volume 14, pp. 453-460 DATE: 1978

AUTHORS/SOURCES: O. J. "Jud" Strock

TITLE: Telemetry - - - Past, Present, Future

ABSTRACT: On the assumption that "the past is prologue", this paper presents an interesting and revealing look at the telemetry technology of twenty years ago, a comparison of that with the technology of today, and an extrapolation into the future of telemetry. Factors which are examined include the characteristics of telemetry systems, the price per unit of performance, and the applications in which telemetry has been, is being, and likely will be used.

DATA ITEM NO. 2

ENTRY DATE 2 July 1979

DATA TYPE: Trade Journal Article

KEYWORDS: PCM Technology Trends

ORGANIZATION:

REFERENCE NO.: Electronic Design 6, pp. 94-99 DATE: March 15, 1978

AUTHORS/SOURCES: Stan Yalof, President, and Don Gregg, Principal Engineer
Tetrahedron Associates, 7605 Convoy Ct., San Diego, CA 92111

TITLE: Collect Data via Pulse-Code Modulation

ABSTRACT: In a data-acquisition system, analog signals with bandwidths below 5 kHz are often best handled with pulse-code modulation (PCM) techniques. Above 5kHz, other ways to handle analog data, such as direct recording and frequency-modulated recording, have their own advantages, depending on the number of channels, the frequency range of the signals and the required accuracy of the recorded data.

Below 5 kHz, however, PCM offers many advantages: data are stored in digital form, thus guaranteeing accurate reproduction of recorded signals; the signal-to-noise ratio is better than 70 dB (about double that of many FM or direct recording methods); and the accuracy of recorded information is within 0.1% (about an order of magnitude better than most other methods).

DATA ITEM NO. 3
ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper
KEYWORDS: Data Systems Description

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 2, pp. 232-253 DATE: 1966

AUTHORS/SOURCES: H. Himmelblau, et. al.

TITLE: Desired Telemetry System Characteristics for Shock, Vibration,
and Acoustic Measurements

ABSTRACT: For over a decade structural dynamicists and acousticians have registered general dissatisfaction concerning the limitations of telemetry systems, especially the insufficient number of channels and insufficient data bandwidths. To spell out the user's need for present and future telemetry, a representative group of dynamicists was organized under the SAE. Requirements for number of channels per flight, data bandwidths, minimum dynamic range (with stationary and transient data signals considered separately), certain accuracy, phase and other characteristics were established. The subcommittee is hopeful that this information will spur the telemetry community into developing and standardizing on new systems with superior characteristics.

DATA ITEM NO. 4
ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: Onboard Processing

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 13, pp. 113-129 DATE: 1977

AUTHORS/SOURCES: Neil H. Endsley, Kyong H. Lee and Robert H. Maschhoff

TITLE: A Data Acquisition System Featuring On-Board Processing

ABSTRACT: A data acquisition system for the telemetry data on the Technology Development Vehicle (TDV) program is presented. To meet the major experimental objectives of the TDV mission--the collection of high frequency vibration and acoustic data on a re-entry vehicle--required some unusual design approaches.

It is shown that collection of this data requires a great deal of data compression. This was accomplished using a technique of on-board data processing--actually performing the first step of data reduction in flight.

The entire data acquisition system is described in light of the requirements imposed by the data with emphasis on unusual problems and solutions.

Results of ground tests in an anechoic chamber are presented, and a brief discussion of the errors involved in on-board processing is given.

DATA ITEM NO. 5

ENTRY DATE 2 July 1979

DATA TYPE: Professional Journal Article

KEYWORDS: Onboard Processing

ORGANIZATION:

REFERENCE NO.: Space Science Instrumentation DATE: 1977
 Vol. 3, pp. 171-185

AUTHORS/SOURCES: D. Jones

TITLE: Signal Preprocessing on Spacecraft

ABSTRACT: Methods of on-board processing of low frequency plasma-wave signals are discussed with emphasis on the retention of phase information. In particular, on-board auto-correlation, cross-correlation and signal-averaging are considered in some detail. Where only two or three wide-band signals are to be investigated, a digital correlator is singularly advantageous; if the number of signals exceeds three then signal averaging using rotating memories is more practicable. The operation of both methods is illustrated using natural VLF signals recorded on spacecraft and on ground.

DATA ITEM NO. 6
ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: Calibration

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 12, pp. 88-99 DATE: 1976

AUTHORS/SOURCES: E. Grant

TITLE: Calibration of Analog Measurement and Telemetry Systems

ABSTRACT: A basic requirement of modern telemetry and instrumentation is a reference or standard to measure against. A brief survey of early flight tests and missile measurement systems shows the development of analog calibration. Frequency Modulation (fm), telemetry, Pulse Amplitude Modulation (PAM), and commutator calibration will be discussed, as well as measurement resistance calibration comparison and the newer actual instrument stimulation techniques. Factors influencing calibration stability and accuracy will be reviewed with a qualitative discussion of accuracy and frequency of calibration as a function of system requirements and measurement accuracy. Digital techniques and components now allow greater accuracy, stability and miniaturization of calibration systems. Low power Schottkey transistors, transistor logic (TTL) and Complementary Metal-Oxide Semi-conductor (CMOS) circuitry allows ease of design of calibration systems. With these newer calibrators, no measurement system should suffer from a lack of accurate calibration.

DATA ITEM NO. 7

ENTRY DATE 2 July 1979

DATA TYPE: Trade Journal Article

KEYWORDS: A/D Conversion & Multiplexing

ORGANIZATION:

REFERENCE NO.: Electronics, pp. 105-116 DATE: May 10, 1979

AUTHORS/SOURCES: N. Mokhoff

TITLE: Monolithic Approach Bears Fruit in Data Conversion

ABSTRACT: Improved circuit design and processing are boosting chip resolution, though hybrids still yield best performance, says this special report.

DATA ITEM NO. 8

ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: A/D Conversion & Multiplexing

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 14, pp. 855-861 DATE: 1978

AUTHORS/SOURCES: R. N. Constant, C. M. Lekven

TITLE: Analog-Digital LSI on the e^{+t} Curve

ABSTRACT: The title of this paper was selected to indicate that large scale integration (LSI) of analog (linear), digital and combined monolithic analog and digital (A & D) circuits for telecommunication system is progressing at an exponential rate. As is the case with exponential functions, near term (i.e., when t is small) increases are rather modest, but, once started, the function grows rapidly. This is the case of A & D LSI: it is just starting to take hold, and impressive gains are expected in the future. The purpose of this paper is to explore, from the system point of view, some of the recent technology developments that have taken place and that are expected to impact the design of future telemetry, communication and sensor equipment.

DATA ITEM NO. 9

ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: A/D Conversion & Multiplexing

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 14, pp. 831-838 DATE: 1978

AUTHORS/SOURCES: L. W. Hobrock

TITLE: High Speed A/D Converter Technology Survey

ABSTRACT: Surveyed are current and future high speed A/D technologies with potential for a significant impact on future systems. Current bipolar silicon monolithic quantizers and hybrid sample-and-hold circuits are described. The gallium arsenide integrated circuit technology, including FETs and TEDs, provides speed increases from 10 to 100. Josephson Junction devices are discussed as a technology potentially offering radical increases in sample rates and reductions in power.

DATA ITEM NO. 10

ENTRY DATE 16 July 1979

DATA TYPE: Professional Journal Article

KEYWORDS: A/D Conversion and Multiplexing

ORGANIZATION: IEEE

REFERENCE NO.: IEEE Transactions on Circuits and Systems, Vol. CAS-25 DATE: July 1978

AUTHORS/SOURCES: Donald T. Corner

TITLE: A Monolithic 12-Bit DAC

ABSTRACT: A monolithic 12-bit digital-to-analog converter (DAC) using thin-film resistors is described. A primary feature is the capability of trimming for linearity after packaging using selective shorting of Zener diodes. Error measurement and trimming algorithms are discussed and an analysis of fundamental error sources is given.

DATA ITEM NO. 11
ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: Analog Signal Processing

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 13, pp. 315-324 DATE: 1977

AUTHORS/SOURCES: G. D. O'Clock, Jr.

TITLE: Comparison of SAW, CTD and Conventional Digital Devices

ABSTRACT: Two solid state technologies, which help to make certain types of signal processors, bandpass filters and matched filters more realizable and practical, will be evaluated and compared in this paper. Both of the technologies of interest have been developing over the past nine years. Both approaches can provide design simplicity, small size and low cost potential on a volume production basis.

DATA ITEM NO. 12

ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: Digital Processing Hardware

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 14, pp. 847-853 DATE: 1978

AUTHORS/SOURCES: W. J. Finn and R. J. Karwoski

TITLE: The Impact of LSI on Telemetry Systems

ABSTRACT: Any system which measures, transmits over a distance, receives, and processes signals can be defined as a telemetry system. Video transmission systems, satellite communications systems wideband data links, and TDM/FDM transmultiplexers all have one thing in common: an increasing need for high-speed digital signal processing. This paper is intended to serve as an introduction to the application of LSI to telemetric signal processors.

DATA ITEM NO. 13
ENTRY DATE 2 July 1979

DATA TYPE: Trade Journal Article

KEYWORDS: Digital Processing Hardware

ORGANIZATION:

REFERENCE NO.: Electronics, pp. 105-110 DATE: March 1, 1979

AUTHORS/SOURCES: M. E. Hoff and Matt Townsend

TITLE: Single-Chip n-MOS Microcomputer Processes Signals in
Real Time

ABSTRACT: Analog inputs and outputs surround high-speed pipelining processor;
user builds filters, oscillators, other analog systems with E-PROM software.

DATA ITEM NO. 14
ENTRY DATE 2 July 1979

DATA TYPE:

Conference Paper

KEYWORDS:

PCM Coding, Recording and Reproducing

ORGANIZATION:

International Telemetering Conference

REFERENCE NO.:

Vol. 12, pp. 526-540

DATE: 1976

AUTHORS/SOURCES: D. A. King

TITLE:

Comparison of PCM Codes for Direct Recording

ABSTRACT: The bit packing performance of randomized-non-return-to-zero (randomized-NRZ), odd parity-NRZ, delay modulation, and bi-phase (Bi-0) in direct recording was experimentally compared at a bit error probability (BEP) of 10^{-6} . The effect of bit patterns, record and reproduce levels, bias level, tape speed, tape recorder bandwidth, bit synchronizers, and crossplay between tape recorders on bit packing density was investigated. At high bit packing densities, significant variations in data quality were found for changes in these parameters. This imposes limitations on practical bit packing densities. Some bit synchronizers were found to seriously reduce bit packing densities. Results show randomized-NRZ to be superior to the other codes in bit packing density.

DATA ITEM NO. 15
ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper
KEYWORDS: PCM Coding, Recording and Reproducing

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 13, pp. 33-51 DATE: 1977

AUTHORS/SOURCES: G. H. Schulze

TITLE: Understanding and Specifying Hi-Density Digital Recording Systems

ABSTRACT: Rapid advancement of hi-density digital recording technology has left most user organizations in a confused and bewildered state with respect to understanding and, more importantly, specifying hi-density hardware either without procurement specifications or with incomplete or shallow specifications will probably gain the needed experience too late, after an unusable system has been delivered. Several prominent user facilities have recently bought and accepted hi-density recording hardware and immediately been forced to retire the equipment from use to avoid disastrous embarrassment. Other users have had to redesign accepted equipment before it could be used. One user who blindly accepted a proposal to convert several newly ordered analog recorders to a digital format had to remove and dispose of the digital electronics after delivery and revert back to analog methods.

The ability to professionally specify and technically monitor a hi-density recording system contract can only be based upon a thorough understanding of the high density digital coding, recording, reproducing and decoding process. The purpose of this paper is to identify and discuss the more important elements of this emerging technology for users who suddenly find themselves needing this capability.

DATA ITEM NO. 16

ENTRY DATE 2 July 1979

DATA TYPE: Conference Paper

KEYWORDS: PCM Coding, Recording and Reproducing

ORGANIZATION: International Telemetering Conference

REFERENCE NO.: Vol. 13, pp. 239-250 DATE: 1977

AUTHORS/SOURCES: E. L. Law

TITLE: Experimental Comparison of Pulse Code Modulation Codes
for Magnetic Recording

ABSTRACT: The bit error probability (BEP) versus signal-to-noise ratio (SNR) was experimentally determined for non-Return-to-Zero-Level (NRZ-L), Bi-Phase-Level (BIL), Delay Modulation (DM) and Miller Squared (M²) codes for a bandpass channel.

DATA ITEM NO. 17

ENTRY DATE 16 July 1979

DATA TYPE: Conference Paper

KEYWORDS: PCM Coding, Recording and Reproducing

ORGANIZATION: International Telemetry Conference (ITC)

REFERENCE NO.: ITC Proceedings, Vol. IX DATE: 1973

AUTHORS/SOURCES: Jon B. Wells

TITLE: High Density PCM Magnetic Tape Recording

ABSTRACT: The Bell & Howell Enhanced-NRZTM recording reproducing technique for bit packing and densities up to 40,000 per track inch is described in this paper. Utilization of the pulse code modulation format of Enhanced-NRZ achieves this high density with a bit error rate of one in ten million. Bell & Howell's standard VR-3700B instrumentation tape recorder and wide-band instrumentation recording tape are used. This same technique permits parallel recording of data rates up to 10 megabits per second at a tape speed of 120 in./s. The merits of the unique encoding/decoding method, factors affecting bit error rate and future opportunities for development are discussed.

DATA ITEM NO. 18

ENTRY DATE 2 July 1979

DATA TYPE: Professional Journal Article

KEYWORDS: Signal and Data Processing Techniques

ORGANIZATION: Institute of Electrical and Electronics Engineers

REFERENCE NO.: IEEE Spectrum DATE: January 1967

AUTHORS/SOURCES: P. I. Richards

TITLE: Computing Reliable Power Spectra

ABSTRACT: Techniques of harmonic analysis have recently crystallized into modern power-spectrum analysis, the presently accepted "best" tool for uncovering periodicities and near-periodicities hidden in noisy data. Despite the simplicity of this concept - to electrical engineers, at least - computing a meaningful power spectrum involves several subtleties that are too easily overlooked by the nonspecialist. This article presents an elementary review of such pitfalls and of their origins.

DATA ITEM NO. 19

ENTRY DATE 2 July 1979

DATA TYPE: Book

KEYWORDS: Signal and Data Processing Techniques

ORGANIZATION:

REFERENCE NO.: Prentice-Hall DATE: 1975

AUTHORS/SOURCES: L. R. Rabiner and B. Gold

TITLE: Theory and Application of Digital Signal Processing

DATA ITEM NO. 20

ENTRY DATE 2 July 1979

DATA TYPE: Book

KEYWORDS: Signal and Data Processing Techniques

ORGANIZATION:

REFERENCE NO.: Wiley-Interscience DATE: 1972

AUTHORS/SOURCES: R. K. Otnes and L. Enochson

TITLE: Digital Time Series Analysis

DATA ITEM NO. 21
ENTRY DATE 16 July 1979

DATA TYPE: NASA Technical Translation

KEYWORDS: Signal and Data Processing Technique

ORGANIZATION: European Space Research Organization Paris

REFERENCE NO.: NASA-TT-F-16544 (NASA 75N31482). DATE: September 1975
Translation of ESRO-SP-99, Proceedings of 3rd Testing
Symposium, Frascati, Italy, October 1973, pp. 581-602
AUTHORS/SOURCES: J. M. Bouquin

TITLE: Acquisition and Digital Processing of Environmental Data

ABSTRACT: The environmental data processed include time variable signals measured on structures subjected to vibrational environments. The data processing consists of two phases: the acquisition phase and the analysis phase. Three types of signal are considered: sinusoidal signals, random signals, and transient signals. Acquisition methods for these signals are presented as well as digital analysis methods which include the digital filtering technique and the Fast Fourier Transformation technique.

DATA ITEM NO. 22

ENTRY DATE 16 July 1979

DATA TYPE: Air Force Technical Report

KEYWORDS: Dynamics Measurement and Analysis

ORGANIZATION: Air Force Flight Dynamics Laboratory, WPAFB, Ohio

REFERENCE NO.: AFFDL-TR-68-42 (NASA 77X72033), DATE: June 1968
DDC AD-847706

AUTHORS/SOURCES: Allan G. Piersol, W. F. Van der Laan

TITLE: Statistical Analysis of Flight Vibration and Acoustic Data

ABSTRACT: Techniques for predicting the vibration environments of future aircraft based upon statistical extrapolations from data measured on past aircraft are investigated. As a first step, principal sources of aircraft vibration are identified, and analytical relationships for the resulting vibration environment are approximated. Available AFFDL data are then summarized and evaluated. Extensive statistical studies are performed on the available data to investigate the average properties of aircraft vibration among the three orthogonal directions, various structural zones, various aircraft models, and various aircraft groups. The available data are also used to study the spatial distribution of vibration levels within a regression analysis procedures to arrive at conservative prediction levels are detailed. The suggested techniques are illustrated using available AFFDL data. Procedures for deriving vibration test specifications based upon environmental vibration predictions are suggested. Finally, possible extension of the techniques to the prediction of internal acoustic noise are discussed.

APPENDIX C

PHASE II INTERIM REPORT

APPLICATION OF PULSE CODE MODULATION (PCM)

TECHNOLOGY TO AIRCRAFT DYNAMICS DATA ACQUISITION

Revision date

Revision letter

Issue date 28 April 1980

Contract number F33615-79-C-3205

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INDEX OF PAGE CHANGES

REVISION DATE AND LETTER	PAGES AFFECTED			REMARKS	REVISED BY	APPROVED
	REVISED	ADDED	REMOVED			

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1. INTRODUCTION

This interim report is being submitted in compliance with Contract Data Requirements List (CDRL) Sequence Number 3 of Attachment Number 1 to Contract F33615-79-C-3205. It covers the contractor's (McDonnell Aircraft Company) work on Phase II (Definition of PCM Systems) of the study authorized by this contract.

1.1 OVERALL STUDY OBJECTIVES

The objectives of this study are to provide AFWAL/FIBG with the following:

- (a) The design of an optimum Pulse Code Modulation (PCM) data acquisition, playback, and analysis system utilizing all, part, or none of the present facility equipment, and
- (b) knowledge of the rationale, considerations, and judgements involved in the creation of that design.

The study involves four phases of effort as follows:

Phase I - Facility Review, Literature Search, Formulation of System Standards and System Goals

Phase II - Definition of PCM Systems

Phase III - Evaluation of PCM Systems

Phase IV - PCM System Design

The results of each phase must be approved by AFWAL/FIBG prior to starting work on the next phase.

1.2 PHASE II OBJECTIVES

- (a) Identify study areas (problems) that have a bearing on the overall system performance and cost.
- (b) Analyze these study areas and form alternate solutions, where possible.
- (c) Continue the literature search, as necessary, in support of (b).

- (d) Formulate candidate systems that have the potential of satisfying the AFWAL/FIBG goals defined in Phase I.
- (e) Perform an evaluation and screening on these systems in order to select the three system configurations to be carried forth into Phase III of the study.
- (f) Present the results of Phase II to AFWAL/FIBG for their concurrence.

2. SUMMARY OF CONCLUSIONS

For design purposes, the overall PCM system desired by AFWAL/FIBG can be divided into the following three subsystems:

- ° Airborne PCM encoder/formatter system
- ° Tape record/reproduce system
- ° Ground system for editing, analysis, and display

Phase II study has resulted in the following;

- (1) A set of characteristics for the airborne PCM encoder/formatter system and eight candidates for same based on the following:
 - (a) Two basic system architectures - one utilizing centralized encoding and formatting, the other a distributed system utilizing remote encoding.
 - (b) Two A/D configurations - one using a dedicated A/D converter per measurand, the other using multiplexed A/D's (one converter per two measurands).
 - (c) Two filter implementations - one using a combination of four analog and two digital filters, the other using four switched capacitor filters and two digital filters per measurand.

All of these systems have the potential of meeting all acquisition goals except those with respect to size, weight, and power requirements. Accuracy, inter-channel phase error, and reliability will require further analysis to determine if these goals can be met.

- (2) With respect to the tape recorder/reproduce system, a set of characteristics necessary to achieve the goals has been formulated; however, no airborne recorder has been found which will meet these requirements. The use of present state of the art recorders will significantly limit either the data bandwidth, the number of data channels, or both.

(3) For the ground editing, analysis, and display system, two candidates have been formulated, each of which has the potential of meeting all applicable goals, except for display throughput. However, the display throughput goal may be met with two electrostatic plotters. One of the candidates is based on a minicomputer, the other on a "super" minicomputer. These candidates allow tradeoffs of initial cost versus editing and analysis throughput.

The airborne system candidates are summarized in Table C-A. Size, weight, and power were computed assuming a single 42 track recorder of the current state of the art (10 1/2" reel, 120 ips). For the transient (continuous sampling) mode at 20-KHz response, this recorder can only handle 72 measurands. By using two such recorders, all the principal goals can be met (except for power, weight, and size). The additional power, weight, and size imposed by the second recorder are 330 watts, 79 pounds, and 2.04 cubic feet.

A summary of the characteristics common to all of the encoder formatter candidates is shown in Table C-B.

A set of tape recorder characteristics that meet the goals are as follows:

- 14" reel size (9200 feet of tape)
- 3 3/4 to 240 ips speed range
- 42 tracks (36 data tracks)

Bit packing density approximately 20.3 kilobits per inch using randomized NRZ-L coding and serial recording.

TABLE C-A
PHASE III CONCLUSIONS, AIRBORNE ACQUISITION SYSTEMS

STANDARD	GOAL	CANDIDATE SYSTEMS CONFIGURATIONS							
		I F A/D	DISTRIBUTED 4VCVS + 2D DEDICATED MUX ADC	I F A/D	DISTRIBUTED 4VCVS + 2D DEDICATED MUX ADC	I F A/D	DISTRIBUTED 4VCVS + 2D DEDICATED MUX ADC	I F A/D	CENTRALIZED 4VCVS + 2D DEDICATED MUX ADC
1. BANDWIDTH/MEASURAND	DC TO 20KHZ	Y							
2. ACCURACY	.5%	P++	+--	-+	--	++	+-	-+	-+
3. ENCODING RESOLUTION	12 BITS PLUS 2 BITS AUTO-RANGE	Y							
4. DYNAMIC RANGE	66 DB PLUS 70 DB AUTO-RANGE	Y							
5. NUMBER OF MEASURANDS	144	Y							
6. INTER-CHANNEL PHASE ERROR	5°	P							
7. RECORD TIME	7.5 MIN. 8.0 HR.	(1) Y							
8. PHYSICAL									
A) SIZE	20 CU. FT.	6.3	6.3	6.3	4.7	4.7	4.7	4.7	4.7
B) WEIGHT	50 LB. N.D.	3.18	3.18	3.18	2.304	2.304	2.304	2.304	2.304
C) MODULARITY	MIL E-54100, CLASS 2	Y							
9. ENVIRONMENTAL CONDITIONS									
10. POWER	112 WATTS @28 VDC	1578	1530	1345	1298	1420	1372	1187	1140
11. RELIABILITY	1000 HRS.	TBD							
12. MAINTAINABILITY	N.D.	(N/D)	-	-	+	-	+	-	+
13. TEST READINESS	N.D.	(T)	+	+	+	-	-	-	-
14. CAPABILITY FOR ON-SITE EVAL.	ALWAYS	Y							
15. OPERATIONAL FLEXIBILITY	N.D.	(T)	+	+	+	-	-	-	-
16. RECURRING MANPOWER SUPPORT	N.D.	(T)	+	+	+	-	-	-	-
17. SYSTEM HARDWARE COSTS	N.D.	TBD							

Y = YES, GOAL ACHIEVED; P = POTENTIALLY FEASIBLE; TBD = TO BE DETERMINED; N.D. = NOT DECLARED;
 (1) ASSUMED TAPE RECORD/REPRODUCER WITH 1/2 TRACKS @ 120 IPS TO OPERATE WITHIN PROPOSED IRIG 106-30
 STANDARD BUT AT 72 MEASURANDS; + MOST DESIRABLE; - LESS DESIRABLE

TABLE C-B
ENCODER/FORMATTER SYSTEM CHARACTERISTICS
MEETING AFWAL/FIBG GOALS

	<u>MODE A (TRANSIENT)</u>	<u>MODE B (STATIONARY)</u>	<u>MODE C (STATIONARY)</u>
NO. OF CHANNELS	144	144	144
FREQUENCY RANGE	DC - 20 KHz	DC - 20 KHz	DC - 20 KHz
TIME UPDATE*	N/A	10.664 SEC	2.664 SEC
RECORD TIME	7.5 MIN	8 HRS	8 HRS
NO. OF BITS/SAMPLE	16	16	16
NO. OF FILTERS SAMPLED	1	6	5
SAMPLES PER CYCLE	3.2768	3.2768	3.278
SAMPLE RATE COMPRESSION RATIO	1	227.5	68.2
SAMPLES PER FILTER PER UPDATE	N/A	64 TO 2048	64 TO 2048

* 512 SAMPLES PER FILTER ASSUMED FOR TIME UPDATE

3. IDENTIFICATION OF STUDY AREAS

3.1 RESULTS

Twenty-two study areas were identified in Phase II:

- (1) Alternate configurations and flexibility of multiple filter encoding.
- (2) Anti-alias filter size and complexity versus sample rate.
- (3) Analog versus digital filter implementation.
- (4) Establishment of recorder bit rate and storage requirements and capabilities.
- (5) Channel and bandwidth capacity versus recording time for stationary and non-stationary acquisition modes.
- (6) Methods of encoding gain status of auto-range signal conditioners.
- (7) Phase matching in acquisition versus phase correction in analysis.
- (8) Data validation (quick-look) at test site.
- (9) Signal conditioning, including automatic gain ranging.
- (10) Sampling and A/D conversion, including sample and hold.
- (11) Transient response of filters.
- (12) Buffer storage and formatting requirements.
- (13) System calibration.
- (14) Remote multiplexing concepts.
- (15) Airborne subsystem size, weight, modularity and power requirements.
- (16) Increased maximum array size for analysis.
- (17) Addition of floating point processing capability.
- (18) Software programming and support equipment requirements.
- (19) Improved plot resolution.
- (20) Data editing methods.
- (21) Merging of analyses from multiple filter data.
- (22) Addition of zoom transform and modal analysis capability.

3.2 DEVELOPMENT OF STUDY AREAS

Specific study areas are indicated in the contract, Reference (1), Sections 4.3.1.1 - 4.3.1.5. The contract also specifies that the list of study areas is to be expanded during the course of the study. Those study areas listed in section 3.1 that were derived from the contract are as follows:

<u>Study Area No.</u>	<u>Contract Reference</u>
13	4.3.1.1
1, 3, 21	4.3.1.2a
6, 9	4.3.1.2b
2	4.3.1.2c
4, 5	4.3.1.2d
8	4.3.1.3
20	4.3.1.4
17, 7	4.3.1.5

During Phase I the existing AFWAL/FIBG capabilities for data acquisition analysis, and display were evaluated, and corresponding goals were established for a new system using PCM. Highlights of desired improvements are as follows:

Data Acquisition

- ° Increased accuracy
- ° Increased dynamic range
- ° Increased number of channels acquired simultaneously
- ° Increased record time
- ° Decreased volume, weight
- ° Improved provisions for data validation at test site

Data Analysis

- ° Capability for modal analysis
- ° Capability for zoom transform
- ° Increased array size

- ° Floating point processing
- ° Increased edit capability

Display Process

- ° Increased resolution

Of particular note are the dramatic increases in efficiencies in airborne volume, weight, and power used for the acquisition system:

AFWAL/FIBG Present WBFM/PAM System	Desired For PCM System
Cubic Inches per Channel 570	24
Watts per Channel 9.33	0.78
Pounds per Channel 9.17	0.35

Study areas other than those derived from the contract were selected because of the improvements indicated by the goals.

4. COMPONENT/SUBSYSTEM ANALYSIS

This task of the study consisted of confronting each of the study areas defined in Section 3., and formulating system characteristics and alternative solutions, where applicable.

4.1 ALTERNATE CONFIGURATIONS AND FLEXIBILITY OF MULTIPLE FILTER ENCODING

4.1.1 MULTIPLE BANDPASS FILTER ENCODING - Acquiring data from multiple bandpass filters is a possible approach to reducing the sample rate. Using this approach, the frequency spectrum of an incoming signal would be divided up by filters into equal bandwidths, as indicated in Figure C-1, and each filter would be sampled at the same rate for equal time periods. A broadband analysis of the signal could then be constructed by analyzing the output of each filter separately, using "zoom" transform frequency scaling (Reference 13), and combining results.

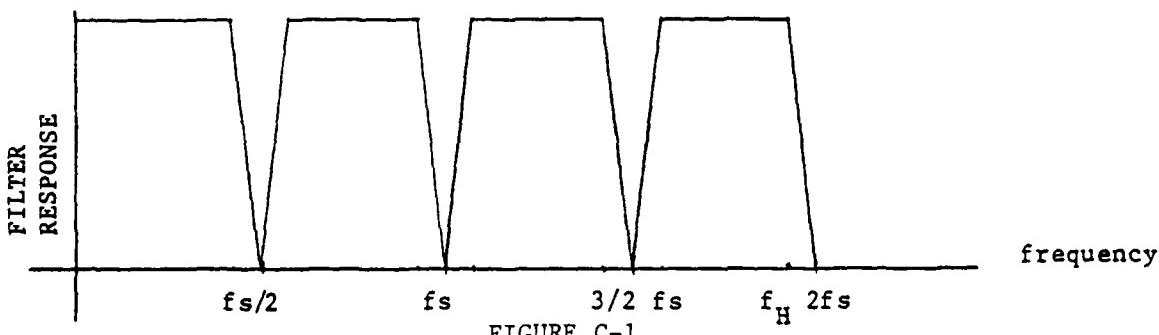


FIGURE C-1

The advantages and disadvantages of this technique (as compared to the multiple low pass filter approach discussed in Section 4.1.2 below) are as follows:

Advantage

- ° Each filter is sampled at the same rate - therefore no buffering of the output samples would be required.

Disadvantages

- ° The sample rate compression achieved is equal only to the number of filters employed. Thus, ten filters are required to reduce the sample rate by an

order of magnitude.

- All but possibly one of the filters would be bandpass rather than lowpass. Bandpass filters are more complex (and hence larger) than lowpass filters of equivalent performance.
- A loss of data would occur in the transition regions of the filters, since the response of all filters would have to be near zero at integer multiples of half the sampling frequency (Reference Figure C-1).

The latter disadvantage could possibly be overcome by employing another set of filters and another sample rate to pick up the data lost in the transition regions of the first set of filters. However, this would even further reduce the efficiency of the method (i.e., the use of ten filters might only cut the overall sample rate by a factor of three or so).

In conclusion, the multiple bandpass filter approach is not a practical technique for achieving a worthwhile sample rate compression where a complete baseband analysis (extending down to, or near, zero frequency) is required.

4.1.2 MULTIPLE LOWPASS FILTER ENCODING - With this approach, the frequency spectrum of an incoming signal is divided up using lowpass filters with cutoff frequencies spaced some constant number of octaves apart. Each filter is sampled, by an A/D converter at a rate appropriate to the filter cutoff frequency and roll off characteristics, for a time duration inversely proportional to the cutoff frequency. This results in an equal number of sample points taken from each filter during each "update", or cycle through the full set of filters. By using a buffer memory to hold the output samples as they are generated, then data can be removed from the buffer at a rate equal to the time weighted average of the individual sample rates.

This rate is, in general, much lower than the rate required for continuous sampling of the highest frequency filter. Thus, data is gathered for analysis

of the entire frequency spectrum at a compressed rate.

Equations have been derived for the compression ratio, time update, and buffer storage, assuming sequential (non-overlapped) sampling of the various filters, and equivalent characteristics for each filter. (Sequential sampling provides slightly more compression than overlapped sampling and is simpler, both from an implementation standpoint and in interpreting editing and analysis results.)

For the equations that appear below, the following definitions hold:

f_H = Highest frequency of analysis, which is the highest filter cutoff frequency.

K_1 = Ratio of sample rate to filter cutoff frequency (assumed equal for all filters).

n = Number of low pass filters employed.

D = Decimation ratio or ratio of sample rates of successive lowpass filters.

N = Number of samples taken from each filter during each update of the filter set.

C = Compression ratio, or ratio of the sample rate of the highest filter to the average rate at the buffer output.

T_u = Time update, or the time it takes to gather N samples from all filters, one time.

M = Buffer memory size (per measurand) required prior to the recorder.

L_t = Total number of lines of resolution resulting from merged fast Fourier transform analyses of the filter outputs. (Note: The lines are not equally spaced, except between filter cutoff frequencies.)

Compression Ratio

$$C = \frac{D^n - 1}{n(D-1)} \quad (1)$$

Time Update

$$T_u = \frac{N(D^n - 1)}{K_1 f_H (D-1)} \quad (2)$$

Buffer Storage

$$M = \frac{N}{2} \sum_{k=0}^{n-1} \left| 1 - \frac{D^k}{C} \right| \quad (3)$$

Total number of lines resolution

$$L_t \approx \frac{N}{K_1} \left[1 + (n - 1) \left(1 - \frac{1}{D} \right) \right] \quad (4)$$

The multiple low-pass encoding method is restricted for use where the overall data signal can be considered stationary for at least two or three update periods of T_u in length.

Plots of the compression ratio (C) and normalized number of lines resolution ($L_t / f_H T_u$) are shown in Figures C-2 and C-3, respectively. By comparing these plots, it can be seen that the higher the compression ratio, the less frequency resolution is available from a given data time length. Or, equivalently, it takes a longer time update period to achieve a given number of lines resolution with a high compression ratio.

Five basic configurations, or filter sets, were conceived as alternatives for study. The characteristics of these configurations are summarized in Table C-1. Each configuration is considered to be a set of low-pass filters (analog and/or digital) connected to each measurand channel in such a way that data from selected filters (all, some, or only one, depending on test requirements) could be sampled and inserted in the PCM stream. For stationary random data acquisition, one of the multiple filter operating modes would be selected, while for non-stationary data, a single filter of suitable response would be selected. All of the configurations, designated 1A - 5A, feature maximum frequency response up to 20 KHz. An alternate set of filter configurations, designated 1B - 5B, was also developed - these feature maximum response to only 10-KHz. Since the stated goal of the study is for 20-Khz response, 1B - 5B are considered "backup" configurations.

Configuration 3A (six filters, with cutoff frequency spacing two octaves apart) has been selected for detailed study. The discarded choices used 4, 8, and 12 filters. Configuration 4A (8 filters) was discarded immediately because it is incompatible with a digital filter implementation approach (sample rates from the various filters are not integer multiples of each other). The remaining choices using 4 and 12 filters were eliminated so as not to bias the study in favor of either an all analog or all digital filter approach.

Detailed characteristics of various conceivable operating modes of configuration 3A are displayed in Table C-2.

4.2 ANTI-ALIAS FILTER SIZE AND COMPLEXITY VERSUS SAMPLE RATE

The anti-alias filter design is basically a trade-off of the filter complexity versus the sampling rate. With the large amount of 20-Khz data sources, the reduction of the sampling rate has a very significant impact upon the A/D converters, the tape recorder and the buffer storage and formatter requirements.

At the same time, increasing the hardware and the complexity of the 144 anti-aliasing filters adds substantially to the size, weight, power and cost of the PCM system. The optimum filter characteristic would provide complete elimination of unwanted frequency components in the sampled data. In order to effectively eliminate noise and not generate the frequency folding phenomena, either sharp cutoff filters or high sampling rates must be provided.

The study considered several types of anti-aliasing filters among which were Bessel, Butterworth, Transitional, Chebyshev and Elliptic. From performance evaluation, the sharper cutoff filters - Chebyshev and Elliptic - provide the best results with reasonable filter orders. The implementation of Elliptic filters is considerably different due to the presence of zeroes in the transfer function having only poles. Although the Chebyshev filter does not provide the sharpness in cutoff for the same filter order as the Elliptic filter, the hardware requirements are less. To achieve equivalent cutoff characterization of the Elliptic filter, a higher order Chebyshev filter is required. The end result is that about the same amount of hardware is required for Chebyshev or Elliptic filters with each type having approximately equivalent cutoff characteristics. The Chebyshev filter then becomes the best filter choice due to its relative ease of implementation.

In order to meet the dynamic range goal (66 dB), frequencies that could cause alias errors in the range of interest (DC up to the filter cutoff frequency) must be rejected by at least 66 dB. For a given sample rate (f_s) and cutoff frequency (f_H), the lowest frequency that has an alias in the range $[0, f_H]$ is simply $f_s - f_H$.

The passband error specification allowed in the definition of frequency response (Reference 4, page 148) is ± 1 dB referenced to the system gain at DC, exclusive of the transducer. Allowing some safety margin for systems employing

one or more cascaded filters (where passband errors of individual filters are additive), the maximum allowable passband error was set at $\pm .5$ dB or 1.0 dB peak to peak.

Figure C-4 indicates the normalized sample rate (samples per cycle of f_H) versus filter order (no. of poles) for Chebyshev filters with .1 dB and 1 dB peak to peak passband error between DC and f_H , and 66 dB rejection at $f_S - f_H$. These curves are based on the theoretical transfer function characteristics of the Chebyshev filter. The curves indicate that a substantial reduction in sampling rate is possible by using moderately high order filters (5 to 8 poles) whereas a point of diminishing return is reached above around 8 poles where additional filter complexity does not permit much reduction in sampling rate.

Table C-3 summarizes the relative size and power requirements for implementation of 5 to 8 pole active Chebyshev filters, using the Voltage-Controlled Voltage Source (VCVS) configuration (Reference 30). This chart indicates that only a small size increase is involved in going from 6 to 7 poles, with no increase in power. Referring to Figure C-4, we find that a very convenient sampling rate (3.2768 samples per cycle, corresponding to 65,536 samples per second at 20 KHz) is compatible with the 7-pole filters. This operating point was thus selected for proceeding with the study. Characteristics of the various PCM system operating modes, based on the selected basic sample rate (65,536 Hz) are shown in Table C-4.

4.3 ANALOG VERSUS DIGITAL FILTER IMPLEMENTATION

The requirement for six filters per measurand (including the anti-alias filter) and 144 measurand channels results in 864 filters in the airborne data acquisition system. All of the filters need to have the same degree of rolloff sharpness in order that the samples per cycle factor (K_1) be the same for all filters (this has been assumed throughout the study). Thus, it is extremely

important to find an optimum realization for the filters in terms of size and power requirements. Analog low-pass filters tend to grow larger as the cutoff frequency is reduced because of the physically larger passive components involved. On the other hand, digital filters require less power and weight at the lower cutoff frequencies, because the arithmetic hardware can be time-shared to a greater degree at low sampling rates. The results of this study area are that the two lowest cutoff frequency filters (19.5 Hz and 78.1 Hz) should be implemented using finite-impulse response (FIR) digital filters, while the four highest filters (20 KHz, 5 KHz, 1.25 KHz, and 312.5 Hz) should be implemented either with VCVS analog or switched-capacitor filters (SCF's).

4.3.1 MULTIPLE ANALOG FILTERS

The implementation of the multiple low-pass filters using analog type filters is shown in Figure C-5. The filters are driven from a signal conditioning amplifier. Each filter output is sampled through a common multiplexer and sample and hold circuits. The requirement for simultaneous sampling of all channels make it necessary to have 6 filters, a filter mux and a sample and hold for each of the 144 channels.

The type of filter best suited to the multiple filter concept is basically the same as the anti-aliasing filter. Sharp cutoff, good passband and stopband characteristics, predictable phase response and good stability are important characteristics of the low-pass filters. The Chebyshev filter was selected as the best compromise filter type for the multiple analog filters. Five, six, and seven-pole filters were considered for the multiple filter application, prior to selection of the seven-pole anti-alias filter in study area No. 2.

The implementation of the Chebyshev low-pass filter was evaluated using three techniques: positive gain VCVS, multiple-feedback, and state variable. The VCVS configuration was selected principally because of its simplicity. Although the VCVS configuration is not the best performer, it has considerably

less parts, exhibits the least amount of offset and requires less bandwidth in the operational amplifiers. Furthermore, its sensitivity to parameter drift is primarily a function of drift in the passive components, not in the amplifiers which are more difficult to screen and predict.

A preliminary design of the low-pass filters indicated three basic sizes which are related to cutoff frequency. A summary of the filter characteristics are shown in Table C-5 for 5, 6, and 7-pole Chebyshev filters. Sizes are shown versus filter orders and cutoff frequency.

4.3.2 DEFINITION OF DIGITAL FILTER CHARACTERISTICS

Figure C-6 shows the results of comparison of the two basic types of digital filters (infinite impulse response IIR and finite impulse response, FIR) as applied to an implementation of the selected multiple filter encoding configuration. The basis for comparison is the overall multiplication rate, which is a measure of the amount of hardware required to implement the filters. An analog anti-alias filter with a cutoff frequency of 20 KHz was assumed, with the remaining five filters implemented digitally. For the IIR filters, elliptic designs were assumed, while for FIR filters "optimal" designs (Reference 14) were assumed, with direct implementation as described in Reference 15. The FIR filter weights were assumed to be represented by 16 bit numbers. The estimated number of FIR filter weights required in order to meet the study goals is indicated in Figure C-7 as a function of sample rate for both 15 and 16 bit weights. Fifteen bits is the minimum number required to attain 66 dB stopband rejection for sample rates greater than 2.86 samples per cycle. Sixteen bits is the minimum number required for sample rates between 2.46 and 2.86 samples per cycle. (Note: the number of bits used here includes a sign bit.)

The comparison of the two digital filter types (Figure C-6) clearly indicates that the FIR filters are superior to the IIR for this application.

The filter arithmetic to be performed is described by the following equation, assuming a linear phase filter with an even number of weights:

$$y(r) = \sum_{i=1}^{\frac{M}{2}} C_i [x(rD-i+M) + x(rD+i-1)] \quad (5)$$

where $y(r)$ = decimated output

$x(n)$ = filter input

M = number of weights (only $\frac{M}{2}$ are unique)

C_i = filter weights

D = decimation factor (equals 4 for the selected multiple filter configuration)

At the selected sample rate (3.2768 samples per cycle) a minimum of 58 16-bit weights are required to achieve the desired filter specifications.

It may be desirable from an implementation standpoint to have an integer number of multiplications per input sample. Since, in the above equation, there are $M/2$ multiplications per output sample and $M/2D$ multiplications per input sample, an integer number of multiplications per input sample would require that M be an integer multiple of $2D$. This means that in this case 64 weights may be preferred.

In order to have some confidence that the desired specifications could be achieved, a 64 weight filter was designed for this application, and the weights were rounded to 16 bits, and the frequency response was computed. The output of the Parks & McClellan design program (Reference 14) for optimal FIR filters shown in Table C-6. The rounded weights are listed in Table C-7, and the frequency response plot is shown in Figure C-8. The response is well within specifications.

4.3.3 DIGITAL FILTER IMPLEMENTATION

Implementing the multiple filters with digital filters requires 5 low pass digital filters following the anti-alias filter. By combining the analog and digital techniques, the number of digital filter stages can be reduced by substitution of analog filters. The following discussion considers the digital and combination analog and digital techniques. Figures C-9 and C-10 are conceptual block diagrams for the two techniques. Each digital filter performs arithmetic operations on 58 or more previous input samples using 16 bit signed coefficients from a PROM. The number 58 has been calculated to be the minimum acceptable number of weights to achieve the desired filter quality goals. The arithmetic consists of 29 multiplications and 58 additions for each output sample. Multiplications are the speed limiting factor (additions are faster and may be performed in parallel with the multiplication process). Table C-8 gives the multiplication rates and memory requirements.

The digital filter technique requires a high multiplication rate as well as a high memory access rate. In order for the digital technique to be at all attractive, there must be substantial timesharing of hardware resources such as multipliers, RAM, and coefficient PROM. One set of multiplier hardware and one set of RAM should be used to implement as many digital filters as possible and as many channels as possible; therefore, the multiplier should be very fast and the RAM should be organized in as large a set as possible consistent with access time and control requirements. A search of available high speed multipliers reveals that 16 by 16 bit two's complement multiplication can be done in no less than about 180 ns over the full temperature range required. A more realistic value considering propagation delays and setup times is about 190 to 200 ns per multiplication. This is equivalent to between 5.0 and 5.3 million multiplications per second. For the purpose of the following calculations, a very optimistic

value of 6 million will be used. (It seems reasonable this rate will likely be achieved in the near future). Although it is certainly possible to perform 16 bit multiplications faster than this using ECL, the substantial increase in IC real estate and power required by MSI ECL make this approach not feasible at present. (Future developments in LSI ECL will probably change the above).

The relevant questions are how many complete channels can be implemented using one 6 million operation per second multiplier? How much RAM will be associated with the multiplier and how fast must it be? Table C-9 summarizes the calculations. Examination of the power requirements for available RAMS's and multipliers leads to calculations presented in Table C-10. The righthand column estimates for minimum total power are probably slightly lower than what could be actually realized with hardware available right now. Table C-11 shows estimates of the requirements for PC board area.

In summary, the following conclusions can be drawn from Tables C-10 and C-11. Board real estate does not appear to be an insurmountable problem of any of the systems described. The largest system will fit on 3 or 4 ten-by-twelve inch multilayer printed-circuit boards. The three smallest systems will easily fit on one such board. What weighs most heavily in determining the feasibility of using a digital filter approach is power consumption. The all digital filter approach (System A) requires an absurd amount of power. The stated goal for total power consumption of the entire PCM system is 112 watts @ 28 VDC. Assumption of even a 70% efficient system supply yields 79 watts of useful DC power for the entire PCM system. On the basis of this available amount of power, systems B, C, and D may be rejected. Systems B and C alone exceed the maximum and system D would allow only about 18 watts left for the implementation of all other subsystems. Systems E and F are marginal and may or may not be feasible depending on the total power required by all other subsystems. Systems G, H,

and I are reasonable in their power requirements and merit serious comparison with other filter techniques.

4.3.4 OTHER FILTERS

There are several other techniques of implementing low-pass filters besides the traditional analog and digital techniques presented in the previous sections. Two relatively new devices are on the market that have considerable potential for application in the multiple filter sampling scheme. The two devices are the Intel 2920 "analog" microprocessor and the Reticon R5600 series switched capacitor filters. Both devices accept analog signals, perform basically digital or switching action on the signal and provide an analog output.

The Intel 2920 device consists of a moderate speed 9 bit A/D converter, a special purpose microprocessor, and an output 9 bit D/A converter. The device can provide low-pass filter operation in the same manner as the classical digital filter except the conversion from analog to digital and the reconversion from digital to analog is contained on the same chip as the digital filter. The 2920 can implement both recursive (IIR) and non-recursive (FIR) filters using classical digital techniques. The device drawback for use in the PCM system is the lack of high resolution encoding (9 bits) and the limited sampling rate.

The Reticon device uses a totally different technique in the realization of filter characteristics. The Reticon device employs a method of simulating resistors with switched capacitors, the theory being that switching an increment of charge through a capacitor at a known rate emulates the flow of current through a resistor. Therefore, the R5600 series devices are configured as standard filters using typical active filter design techniques. Another feature of the Reticon filter is the high sampling rate capability which alleviates the requirements for anti-aliasing filters. From a size and power consideration

the Reticon filter is unsurpassed, since it provides a complete filter in a single DIP package. The drawback to the Reticon filter is the lack of experience with the device. Offset voltages, temperature range, and noise characteristics need to be tested before any commitment is made. However, the filter has enough potential that it must be considered as a candidate once the system configuration has been defined.

4.4 ESTABLISHMENT OF RECORDER BIT RATE AND STORAGE REQUIREMENTS AND CAPABILITIES

Table C-3 indicates the bit rate and storage requirements of the various operating modes of the system. The requirements for the modes that meet the goal of 20-KHz response are as follows for 144 measurands:

<u>MODE</u>	<u>BIT RATE</u> <u>MBITS/SEC</u>	<u>STORAGE</u>
A	150.995	6.79×10^{10} (7.5 MIN)
B	0.6637	1.91×10^{10} (8 HRS)
C	2.2140	6.38×10^{10} (8 HRS)

These requirements are based on 16 bit samples (Reference section 4.6) and do not include any overhead words needed for synchronization, time reference, etc.

It was determined in a previous MCAIR study (Reference 16) that magnetic tape recording probably will remain the only practical airborne storage device in the foreseeable future for bit storage on the order of $10^9 - 10^{10}$.

Digital magnetic recording can be performed with either serial or parallel techniques, although serial recording is preferable for this application. Parallel recording is more appropriate in cases where there is a single high bit rate source which must be distributed among a number of tape tracks to alleviate the bit packing density. In this application there are up to 144 independent data sources. From a reliability standpoint, with serial recording

of a few measurands per track, the failure of single record amplifier or tape track would not be catastrophic as it would be in parallel recording with all measurands involved in all tape tracks.

Another argument for serial recording is that newly proposed IRIG standards (Reference 21) have endorsed serial recording, while postponing consideration of parallel recording.

Finally, from a cost standpoint, serial recording offers a better chance of reusing AFWAL/FIBG existing Honeywell 96 laboratory recorder/reproducers.

In order to span the range of recording times from 7.5 minutes to 8 hrs, either of the following recorder characteristics are required, assuming standard 1 mil nominal tape thickness:

<u>REEL SIZE</u>	<u>TAPE LENGTH</u>	<u>SPEED RANGE</u>
10 1/2"	4600 ft	1 7/8 - 120 i.p.s.
14"	9200 ft	3 3/4 - 240 i.p.s.

Figures C-11 and C-12 indicate the number of tracks versus bit packing density per track for the three 20-KHz PCM modes for each of the above sets of recorder characteristics. Note that for equal formatting on each track (constant number of measurands per track for 144 measurands), the maximum number of tracks available with standard head configurations is as follows:

<u>STANDARD HEAD NO. OF TRACKS</u>	<u>MAXIMUM NO. OF DATA TRACKS</u>	<u>NO. OF MEASURANDS PER TRACK</u>
14	12	12
28	24	6
42	36	4

The figures indicate that only the 14" reel size recorder with 240 ips speed is capable of meeting the goals within the current industry standard of 33 kilobits per inch packing density. Additionally, in order to keep the density within the proposed IRIG limit of 25 kilobits per inch using randomized NRZ-L code, a 42-track head configuration is required.

Capabilities of current airborne recorders and portable and laboratory recorders are summarized in Tables C-12 and C-13.

4.5 CHANNEL AND BANDWIDTH CAPACITY VERSUS RECORDING TIME FOR STATIONARY AND NON-STATIONARY ACQUISITION MODES

Based on the use of a recorder that will meet the record time goals for 20-KHz data the following record time will be available for the non-stationary (continuous sampling) acquisition modes:

<u>MODE</u>	<u>FREQUENCY RESPONSE</u>	<u>RECORD TIME</u>
A	20 KHz	7.5 MIN
D	5 KHz	30 MIN
G	1.25 KHz	2 HRS
J	312.5 Hz	8 HRS
K	78.1 Hz	8 HRS
L	19.5 Hz	8 HRS

Stationary acquisition modes will be limited to 8 hours record time by the recorder reel size.

4.6 METHODS OF ENCODING GAIN STATUS OF AUTO RANGE SIGNAL CONDITIONERS

One method of recording gain status of auto-range amplifiers is the one currently in use by AFWAL/FIBG, that is, to record the gain values as separate entities from the data on separate tape tracks. This is necessary in the

present analog data recording system; however, other methods more convenient for editing and analysis can be employed with a PCM system.

Twelve bits are required for data encoding in order to satisfy the goals. Three bits are required to represent the eight different gains of the auto range amplifiers. By designing the PCM system with 16 bit data words, the gain code can be allowed to appear in every word, with one spare bit. This is very convenient for data entry to the ground computer system, and allows for possible interfacing with aircraft onboard mission computer data which conventionally employs 16 bit/word encoding.

4.7 PHASE MATCHING IN ACQUISITION VERSUS PHASE CORRECTION IN ANALYSIS

For single channel analyses such as auto-PSD's, one-third octave RMS, auto-correlation, probability densities, etc., phase matching from channel to channel is of no concern. However, phase matching is important for two-channel analyses such as cross-correlation, cross PSD's, and transfer functions.

One exception is the coherence function for which phase matching is not nearly as critical; however, long time delays (several sample periods) of one channel with respect to the other can cause a bias in the coherence estimate - Reference (4).

In a PCM system there are two basic causes of phase mismatch between channels. One is mismatch of phase characteristics of analog circuitry (primarily filters) and the other is a time delay in sampling from channel to channel. The latter causes a linear phase shift in cross PSD's and transfer functions which can be corrected in the analysis, assuming the time delay is known. The phase correction to be added to the computed phase angle is as follows:

$$\phi_c \text{ (degrees)} = 360 f T_d \quad (6)$$

where f = frequency

and T_d = time delay between channels (positive if "output" channel lags "input" or reference channel)

For cross-correlation analysis, the correction consists of offsetting the lag time axis to account for the time difference between corresponding samples.

Phase mismatch of analog circuitry is not predictable - correction in this case would require calibration. This would be difficult to do, especially in changing environmental conditions. It would be preferable to use filters with phase characteristics that are matched and that track with temperature changes.

The goal for inter-channel phase error is 5 degrees, maximum at 10 KHz, exclusive of known fixed time delays that are corrected in the analysis. Therefore, .5° at 10 KHz can be considered a negligible phase error due to time delay. This corresponds to 140 nsec - the maximum time delay in sampling any two channels before correction in analysis is deemed necessary.

4.8 DATA VALIDATION (QUICK-LOOK) AT TEST SITE

Alternative solutions to this problem are:

- ° Provide a tape playback machine and bit synchronizer at the test site. This will allow verification that a PCM wavetrain was recorded on each track.
- ° Provide a tape playback machine, bit synchronizer, and a decommutation system with word selector. This will allow inspection of individual data words.
- ° Provide a tape playback machine, a decommutation system, and a set of D/A converters and a scope or strip chart recorder. This will allow evaluation of data levels of individual words.

4.9 SIGNAL CONDITIONING, INCLUDING AUTOMATIC GAIN RANGING

Signal Conditioning for the PCM system is primarily a function of providing adequate system gain to accurately measure the vibration and acoustic transducers. These transducers are characterized by very wide dynamic measurement ranges (in excess of 140 dB) which can only realistically be measured with some form of variable gain. Both the vibration and the acoustic transducers require high input impedance buffering to prevent loading errors. The low amplitude level of the output signals also dictate the use of differential signal conditioning to reject common mode noise voltages.

Other types of transducers (strain gauges, thermocouples, RTD's, etc.) can be obtained with their own self-contained signal conditioning. Such conditioning circuitry consists of bridge completion networks, reference junctions, constant voltage or constant current excitation supplies. However, these forms of signal conditioning are unique to particular transducers and are more appropriately provided either in the transducer assembly or as separate signal conditioning units. Except for the vibration and acoustic measurements, most transducers typically do not cover wide dynamic ranges. Where these instances do occur, the gain control feature applies equally as well.

Two methods of providing gain control have been investigated. The two techniques are automatic gain ranging (AGR) and programmable gain (PG) amplifiers. Both techniques have advantages and both are utilized in PCM systems at this time.

The AGR amplifier technique is more recently applied in PCM systems, although this technique has been used in digital voltmeters for several years. However, the speed of sampling in PCM systems makes implementation of high speed auto ranging a very complex problem. The auto ranging concept has several outstanding features of which the most obvious are the ease with which the measurements can be made and the large dynamic gain ranges. Prior knowledge of the signal characteristics and expected outputs are not as critical as with a preadjusted or programmed gain system. Storage hardware is not required for gain level control. Quick substitution of transducer types is possible without the need for program changes.

The AGR amplifier also has some rather serious drawbacks. One of the major disadvantages of an autoranging system is the bit overhead penalty required in keeping the gain setting with the PCM data. Programmed gain systems eliminate the bit overhead since each data measurement has been obtained at a

known gain setting. For high speed systems, the extra burden of recording gain bits with each data word is a significant problem. Another disadvantage of the AGR technique is the additional hardware required to perform the gain control operation. The impact of this additional control hardware is somewhat offset, however, by the lack of programmed gain storage.

While AGR amplifiers are not widely used in PCM systems, PG amplifiers are very commonplace. Most PCM systems designed within the past ten years incorporate programmed gain control. PG amplifier systems are less complex than gain ranging. They are better adapted to multiplexed and high speed configurations since gain setting determination is already preselected. Calibration of PG amplifiers is somewhat improved since the gain selection mechanism is already present and can be utilized to optimize the calibration gain. The PG system has complete control of the gain setting which may be advantageous in some measurements.

Disadvantages of the programmable gain as compared to the auto gain ranging are primarily in the extra effort involved in programming the system for each measurand and the practical limitation of gain changes within a program. Present day PG systems are not "in flight" adaptive in that each measurand is determined at a programmed gain setting, which remains constant throughout the format. Auto gain ranging systems, on the other hand, can provide the full dynamic gain limits for each measurand within the format. Thus a PG system could provide only a single optimum gain setting for a transducer while an AGR system can cover the min to max gain setting provided in the amplifier.

A brief comparison of AGR amplifier and the PG amplifier is shown in Table C-14. Both amplifiers will satisfy the systems accuracy and response. However, only the AGR amplifier can provide the full 70 dB dynamic range. Thus, use of the PG amplifier can be considered only when measurands do not exceed

the programmed limit.

4.10 SAMPLING AND A/D CONVERSION, INCLUDING SAMPLE AND HOLD

4.10.1 SAMPLE AND HOLD REQUIREMENTS - All sampled data measurement systems have an uncertainty error voltage due to the change in input signal during the A/D conversion. This uncertainty error has historically been referred to as aperture error and the time of uncertainty in the measurement process as the aperture time. Although there are many factors which contribute to aperture error, the two most significant factors are the rate of change of input signal and the time during which this signal is sampled and encoded. The rate of change of the signal for a 20-KHz sinusoid is a maximum of $0.1257 E_p$ volts/ μ sec where E_p is the peak voltage. Assuming a full scale signal of E_p peak, a 1 μ sec uncertainty in sampling would yield a possible error of 12.7%. The fastest A/D converters that could realistically be used in an aircraft environment can encode in approximately 100 nanoseconds. This would result in a maximum aperture error of 1.26%. The 100 nanosecond encode time is achieved by utilizing a parallel encoder configuration and is quite complex. A/D converters which utilize successive approximation techniques can operate at 100 to 200 nsec per bit, which for 12 bit resolution would yield 1.2 to 2.4 μ sec encode time.

The sample and hold technique will provide significant improvement in the reduction of aperture error and allow the utilization of a less complex A/D converter. The aperture error of a sample and hold configuration is a function basically of the speed with which the circuit can switch from the sample mode to the hold mode and the amount of jitter in the PCM clock system. It is possible to configure sample and hold circuits with aperture switch times of 10 to 20 nsec. Clock jitter can likewise be controlled to within 20 nsec so that a cumulative aperture time of 10 to 40 nsec can be achieved. Improvement in this

performance can be obtained with ultra high speed hybrid configurations at considerable complexity and expense. With an aperture time of 40 nsec, the maximum uncertainty error is 0.5% using the previous example. Ultra high speed hybrid sample and hold can reduce the switch aperture time to less than 100 ps. Thus, the PCM clock jitter would establish the performance time.

In the trade off of system performance and costs, the sample and hold complexity and the A/D converter complexity can be greatly influenced by the allowable aperture error. The graph in Figure C-13 shows the error due to aperture times as a function of signal frequency. Sample and hold circuit comparisons are shown in Table C-15 for typical monolithic integrated circuitry, a configuration developed with discrete components and an ultra high speed hybrid unit.

4.10.2 ANALOG TO DIGITAL IMPLEMENTATION - Implementation of the analog to digital conversion process, considering present technology, is pretty much restricted to successive approximation techniques or parallel encoding techniques. Both methods are well tested and have in the past few years been greatly improved with the introduction of new monolithic devices. Successive approximation encoding is performed at 0.1 μ sec to 10 μ sec per bit and can be obtained with 14 bit accuracies and up to 16 bit resolution. A general consideration for successive approximation encoders is that 8 to 12 bits resolution can be obtained at 0.1 to 1.0 μ sec per bit. Over 12 bits resolution, the available hardware is generally much slower, principally due to the accuracy requirement in settling the D/A converter and the slow response time of high accuracy comparators.

Parallel encoders have not been utilized in applications requiring more than 6 bits until the recent introduction of monolithic devices from TRW, Advanced Micro Devices, and Texas Instruments. The concept of parallel encoding

requires a comparator for each decision level ($2^n - 1$; where n is the bit resolution). Thus, an 8-bit encoder would require 255 comparators with 255 threshold reference voltages. A 255 line to 8-line logic encoder is then necessary to convert the comparator outputs to the 8-bit code. Each extra bit of resolution effectively doubles the amount of hardware. The new monolithic devices have integrated much of the hardware needed for parallel encoding. The TRW units provide 6, 8, or 10-bit encoders in a single chip LSI packages. Resolution beyond 10 bits is obtained by utilizing a parallel sub ranging technique whereby the encoding is performed in two stages. The sub ranging technique requires, in addition to the parallel encoder, a high speed D/A converter and accompanying control circuitry and has a total encode time approximately three times that required for a single parallel encode operation.

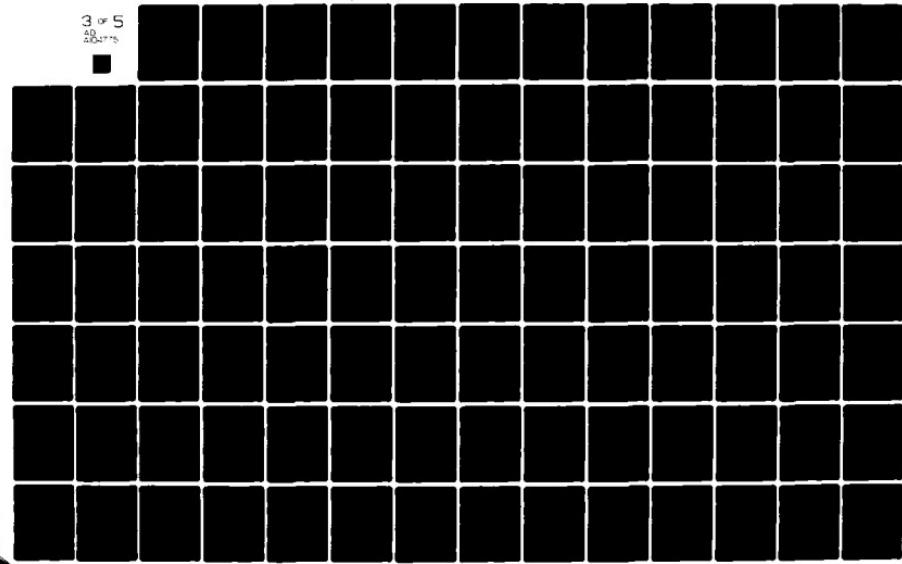
The system goals for the PCM hardware specify 66 dB of dynamic range plus 70 db of gain range, with a maximum sampling rate for any measurand of 60 to 80 KHz. These requirements can be met by either of the two encoding techniques described. The dynamic range of 66 dB is possible with 11 bits resolution plus 1 bit for sign. The encode time of 12.5 to 16.7 usec is easily furnished by either encoding technique. It is possible to utilize one A/D converter for encoding several channels through the use of multiple sample and hold circuits. Maximum utilization of the successive approximation encoder would allow one A/D for approximately 8 to 12 channels. The parallel encoding technique could accommodate approximately 60 to 80 channels. Comparative summaries of both A/D conversion techniques are shown in Table C-16 assuming a 12-bit resolution encoder (11 bits + sign bit). It should be noted that using an A/D converter for several channels necessitates the use of a high speed multiplexer which introduces added hardware and increases data errors. High speed multiplexers (those required to settle in 50 nanoseconds or less) generally are implemented with

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amplifiers and diode bridge switches. This form of implementation requires considerable power and seriously degrades accuracy of the sampled signal. Even though it is possible to multiplex data into a few high speed A/D converters, the increased complexity and degraded performance of high speed multiplexers makes this approach unappealing. It is possible to configure small multiplexers with reasonable accuracy and good settling characteristics where the channel capacity is no more than 8 to 16 channels. The evaluation of configurations will explore the merits of dedicated and multiplexed A/D converter systems.

4.11 TRANSIENT RESPONSE

The transient response of the anti-aliasing and multiple low pass filters must be established to guarantee that the system configuration can handle gain switching and calibration switching operations. The transient response of the analog filters have been determined for a 6 pole Chebyshev configuration were a 6 pole filter to be employed. The settling error of the filter versus the ratio of switching time to filter time constant is shown in Figure C-14. The transient response of the digital filters is shown as follows:

1st digital filter (5 KHz cutoff)	0.855 mS
2nd digital filter (1.25 KHz cutoff)	3.54 mS
3rd digital filter (312.5 Hz cutoff)	14.2 mS
4th digital filter (78.1 Hz cutoff)	56.6 mS
5th digital filter (19.5 Hz cutoff)	227 mS

Maximum transient response time for serial connection of all 5 filters is 302 mS.
Maximum transient response time for serial connection of 4 lowest filters is 301 mS.

Maximum transient response time for serial connection of 3 lowest filters is 298 mS.

Maximum transient response time for serial connection of 2 lowest filters is 284 mS.

The preceding information sets an upper time limit for filter recovery after a gain range change of the auto-gain input amplifier.

4.12 BUFFER STORAGE AND FORMATTING REQUIREMENTS

4.12.1 DATA FORMATTING - Because the data editing and analysis will use data block sizes that are integer powers of two, it is highly desirable to create a format where the number of samples per channel per frame is also a power of two. Current IRIG standards dictate the use of a frame length no longer than 8192 bits or 512 16-bit words.

An estimate of the number of overhead words required in the format is as follows:

2 synchronization words
2 words for frame count
2 words for time code
1 word for data status (filter identification)
1 spare

Total of 8 words overhead per frame

A 264-word PCM frame (256 data words plus 8 overhead) is satisfactory for the 42-track recorder configuration. For the 28-track configuration, a 392-word frame (384 data words plus 8 overhead) is more suitable.

Frame rates for the three primary modes are as follows:

	<u>42 TRACK</u>	<u>28 TRACK</u>
MODE A	1024 FRAMES/SEC	1024 FRAMES/SEC
MODE B	18.004	9.002
MODE C	15.015	15.015

4.12.2 DATA MEMORY REQUIREMENTS - Temporary storage of digitized data from the data channels is required to accumulate high sample rate data while transmitting multi-track formatted data to the tape recorder. The data buffer memory capacity is a function of the number of measurands, the number of filters sampled, and the number of samples per filter per time update, as indicated in Section 4.1.

For Mode A transient data sampling, data memory requirements can be met by a single buffer register per data channel. The multiple filter sampling modes require a data memory storage capacity which is primarily dependent on N, the number of samples per filter per update, and secondarily dependent on n, the number of filters sampled. The buffer storage requirements for Modes B and C are summarized as follows:

<u>N(SAMPLES/FILTER)</u>	<u>M(WORDS/CHANNEL)</u>	<u>M_T(144 CHANNELS)</u>	
64	233	33,552	Mode B (6 Filters)
128	465	66,960	
256	929	133,776	
512	1857	267,408	
1024	3714	534,816	
2048	7427	1,069,488	

<u>N(SAMPLES/FILTER)</u>	<u>M(WORDS/CHANNEL)</u>	<u>M_T(144 CHANNELS)</u>	
64	177	25,488	Mode C (5 Filters)
128	353	50,832	
256	705	101,520	
512	1410	203,040	
1024	2820	406,080	
2048	5640	812,160	

Data memory organization is a function of the data formatting to the tape recorder interface. Assuming a 42-track recorder, Mode B formats 16 measurands per recorder track and utilizes 9 tracks for the maximum data channel capacity of 144 data channels. Mode C recording formats 4 measurands per recorder track and utilizes 36 tracks. A memory organization that segments the data inputs into nine data paths with 16 data channels per data path allows memory cycle times within the range of large capacity dynamic RAM's. With the worst-case total bit capacity required for Mode B sampling of approximately 16 megabits the availability of 64 Kbit dynamic RAM's with cycle times in the 250 to 300 nsec range will determine the upper limit on the number of samples per filter with the full channel capacity of the PCM system being utilized. Utilization of these devices would require more than 250 16-pin RAM's for the worst-case bit capacity listed above. The cycle time allows an ample margin for data write cycles at the higher sample rates, data refresh overhead, and the data memory read rate to the tape recorder interface.

Simultaneous sampling of all data channels permits common addressing logic for the 9 segments of data memory. The formatter provides read and write addresses to the data memory and read data multiplexing for the tape recorder interface.

4.13 CALIBRATION TECHNIQUES

There are two basic calibration techniques applicable to the PCM system which have been investigated. The two techniques are dynamic offset correction and throughput system calibration.

4.13.1 DYNAMIC OFFSET CORRECTION - Dynamic offset correction is a method of eliminating offset and other errors which are variable throughout the operating mission of the PCM system. Most offset errors are a function of the temperature of the unit, however, humidity, aging, voltage, and noise all have contributing effects on offset error. Due to the unpredictable nature of offset error and the magnitude of error changes during a test, some method of periodic error correction is required to maintain overall system accuracy. Typically, most PCM systems using offset error calibration do so by providing a calibration cycle time within the normal sampling format. Analog circuitry in the PCM system is usually calibrated during non-analog sampling portions of the format such as sync and frame I.D. time slots and digital data words. Unfortunately, the high speed PCM system for measuring vibration and acoustic data does not provide convenient times within the format for offset correction cycles. Because of the high sampling rate and the requirement to maintain a constant sampling interval, it is not possible to utilize sync words. Since no digital data is sampled with the PCM system, this normally available calibration time cannot be utilized. The only practical method of calibrating the PCM system is to perform offset correction at those times when data is not being recorded or to suspend the sampling process long enough to allow the system to be calibrated. One opportunity to calibrate is during the several seconds of time allowed for the tape recorder motors to obtain record speed. If a test mission provided several cycles of turning the tape recorder on and off, the calibration operation could be incorporated as part of the recorder settling time. In missions having long

continuous record intervals, the most appropriate calibration method would be short periodic interruptions of the sampling operation to allow calibration.

Those areas of the PCM system that require calibration are the signal conditioning amplifier, the low pass filters, the sample and hold circuit, and the analog to digital converter. Each of these 4 circuit functions has different calibration requirements. The A/D converter is relatively simple to calibrate provided a successive approximation conversion scheme is employed. A correction servo loop can be incorporated in the A/D converter to eliminate the offset errors of the ladder switches, leakage currents, and the comparator offset errors. If the sample and hold circuit is dedicated to a single A/D, then the same correction loop used for the A/D can also be used to eliminate the offset and switching errors of the S/H. If the S/H must share an A/D with several other circuits, then each S/H will require its own offset correction loop. Calibration speed for both the A/D converter and the S/H circuit is relatively fast. The acquisition and hold time of the S/H is no more than 1 or 2 microseconds while the A/D converter can be settled within 200 nanoseconds. It is possible to obtain a calibration cycle in less than 3 microseconds for the two circuits provided the calibration correction loop can be settled. Since the correction loop needs a very long "hold" time constant, most loops employ either a long time constant integrator or an integrate and hold circuit. The correction loop operation is very sensitive to the frequency with which calibration cycles are performed. The more frequent the cycle, the faster the loop response can be made. Thus, it would be possible to calibrate the S/H and A/D just prior to the sampling and encoding of each data point. This method of calibration provides excellent results with a minimum amount of hardware. Furthermore, it can be made a basic function of the converter control logic, thereby, reducing the formatter complexity. This method does require a dedicated A/D or at least

an A/D with sufficient free time to perform a calibration cycle at the highest sampling rate (15.3 microseconds).

The calibration of the signal conditioning amplifier and the low pass filters is considerably more complex than the S/H and A/D circuitry. The settling time of these circuits is so long that it would be impractical to attempt calibration at the normal sampling rate. The only way to provide calibration correction for the signal conditioning amplifier and the low pass filter is to perform the correction prior to sampling data or to interrupt the data sampling periodically. Settling time for the signal conditioning amplifier is approximately 250 to 400 microseconds at the highest gain setting. The filters are much worse requiring over a second to settle for the lowest cutoff frequency. Furthermore, the circuits also require the same time to settle back to the data value as to settle to the calibration value. Because the calibration time for the signal conditioning amplifier and the low pass filters is so long and, therefore, cannot allow frequent calibration cycles, the technique of maintaining correction between calibration cycles becomes a critical design problem. The only practical scheme, thus far, uncovered is to store the correction signal in digital form in a register or memory. The signal conditioning amplifier will require an analog correction voltage which necessitates a D/A converter in the correction loop. The filters may be corrected by either inserting an analog signal into the filter output or by subtracting digitally the correction signal from the digitized data. From a hardware implementation comparison, the digital approach is more efficient. A detailed evaluation of two methods will be presented in Section 6 since each method impacts the calibration hardware of the signal conditioning amplifier and the S/H and A/D.

Once the physical characteristics of the PCM system are established, it will be possible to predict the performance of the calibration operation versus

time between calibration cycles. Using the thermal response of the system as the offset driver, the drift between calibration cycles can be calculated both as a function of time and of environment.

4.13.2 THROUGHPUT SYSTEM CALIBRATION - Throughput system calibration is a method of checking the response of the system to an active stimulus. In the basic concept, a signal having a fixed frequency and amplitude is switched into one or more of the data channels. The signal source is processed in the normal manner and the digitized data is recorded. The results can be used to calibrate the throughput accuracy of the PCM system. The concept can be expanded to allow a variable frequency, variable amplitude signal source which will allow evaluation of phase distortion and gain linearity in addition to accuracy. The throughput calibration can also be combined with a "quick-look" verification test to insure all channels are operational prior to flight tests. The hardware impact of the throughput calibration is mostly in the ground checkout equipment. The PCM system only requires a 2 to 1 multiplexer switch for each channel, which in comparison to the amount of hardware already required, is almost insignificant. The inclusion of the throughput calibration capability is a tradeoff of the slight increase in hardware versus the benefits obtained from real time knowledge of the system performance.

4.14 REMOTE MULTIPLEXING CONCEPTS

Remote multiplexing configurations of the PCM data system require high speed data bus communication between the remote data channel multiplexers and the control unit data formatter. Data bus configurations are a function of the maximum sample rate, the number of data channels per remote unit and the control unit. The system restraints and implementation of parallel and serial bus configurations utilize twisted-pair, shielded cable for the bus, with bi-phase

data rates of 10 to 12 MHz as a realizable goal. In addition, data buffering in the remote units is required for simultaneous data sampling.

4.14.1 PARALLEL BUS IMPLEMENTATION - A parallel bus configuration of a distributed PCM system requires 16 signal lines operating in a half-duplex, command/response mode. At a maximum sample rate of 65,536 sps, the control unit must address and receive data from 144 channels in a period of approximately 15.3 microseconds. The bus format of command and data words is determined by the number of data channels implemented in each remote unit. Assuming 16 channels per remote unit, each sample period would contain 9 command words and 144 data words for a full complement of data channels. The resulting bus data rate is approximately 10 MHz.

The bus command word contains the following control information:

- ° Command Word Flag
- ° Sample Rate Flag
- ° Remote Unit Select
- ° Data word Count
- ° Filter Select
- ° Auto Gain Change Enable
- ° Calibration Cycle Enable

The command word flag is a dedicated bit used by the remote units to distinguish between command words from the controller and data words from other remote units. The parallel bus message protocol contains command words followed by groups of data words from the selected remote unit. The sample rate flag is set in the first command word of a sample period to initiate data channel sampling.

The parallel bus configuration provides flexibility in the number of channels implemented in the remote units. The remote units could be implemented

with channel capacities of 8 to 24 channels with realizable data bus rate. The parallel bus does, however, require 16 signal lines from the control unit to the remote units.

4.14.2 SERIAL BUS IMPLEMENTATION - A serial bus configuration of the PCM system would contain a command bus common to all remote units and a data bus dedicated to each remote unit, operating in a full-duplex mode. The maximum number of data channels per remote unit is determined by the sample rate period of the bandwidth of the data bus. At a sample rate of 65,536 sps, a remote unit configured with 8 data channels would require a data bus bit rate of approximately 9.44 Mbps to transmit buffered data during the current sample period. Since the serial configuration requires bus bit rates directly proportional to the number of channels sampled per remote unit, an 8-channel remote unit is the maximum configuration realizable with the data rate limitations discussed previously.

The serial configuration limits the remote unit channel capacity, but provides cabling convenience to the remote units, since each unit requires only the common serial command bus and a dedicated serial data bus.

4.15 AIRBORNE SUBSYSTEM SIZE, WEIGHT, MODULARITY AND POWER REQUIREMENTS

An analysis of the system goals versus current AFWAL/FIBG capabilities indicates over an order of magnitude improvement in size, power and weight per channel is desired:

	<u>CURRENT</u>	<u>FUTURE</u>
WATTS PER CHANNEL	9.33	0.78
CUBIC INCHES PER CHANNEL	570	24
POUNDS PER CHANNEL	9.17	0.35

4.16 INCREASED MAXIMUM ARRAY SIZE FOR ANALYSIS

The required goal for a maximum input array size of 16,384 16-bit words dictates that the Raytheon 704 array transform processor (ATP) be replaced.

The Raytheon ATP including driver and theta table uses 28K words of 704 CPU memory to accomplish that goal. This leaves only 4K words of storage for running tasks within the 704 CPU.

When the computer precision goal is taken into account requiring 32-bit floating point, the Raytheon ATP would not have enough memory even if it used all of the 32K words of available 704 CPU memory. At least 36K words would be needed just for the ATP.

Current 32-bit array processors provide FFT processing of 1,024 real data points at least an order of magnitude faster than the Raytheon ATP which is 40.8 milliseconds. Anywhere from 312K to 2,432K bytes of memory can be obtained for maximum memory configurations on today's array processors independent of the memory on the host computer.

4.17 ADDITION OF FLOATING POINT PROCESSING (FPP) CAPABILITY

The required goal for 32-bit floating point computer precision determines the Raytheon 704 CPU be replaced because it only has 16-bit fixed point multiply and divide hardware. It is not feasible to depend on software routines to negotiate the throughput requirements for the volume of data potentially in the PCM system.

The table below shows execution times for single (32 bit) precision and double (64 bit) precision arithmetic operations for typical 16-bit and 32-bit word minicomputers today. All floating point today is done with normalization of the mantissa to preserve precision.

Table of Maximum Execution Times with FPP Hardware in Microseconds:

WORD SIZE IN BITS	COMPUTER TYPE	MULTIPLY		ADDITION	
		SINGLE PRECISION 32 BITS	DOUBLE PRECISION 64 BITS	SINGLE PRECISION 32 BITS	DOUBLE PRECISION 64 BITS
16	MEDIUM MINI	13.4	20.7	7.5	7.5
16	LARGE MINI	3.4	6.2	2.5	4.1
16	MICROCODED MINI	1.0	3.6	2	3.6
32	SUPER MINI	1.0	3.4	.8	1.4

4.18 SOFTWARE PROGRAMMING AND SUPPORT EQUIPMENT REQUIREMENTS

Ignoring application programming, the system support programming necessary to build this decommutator ground system requires the following tools:

- ° Macro assembler.
- ° Structured Fortran compiler.
- ° Pascal or Ada compiler or substitute high level systems implementation language.
- ° Complete real time multi-tasking operating system source in machine format for possible operating system customization.
- ° Good system and user manual documentation standards from start of system development.

The system support software programming to negotiate various ground systems is as follows:

- ° Software disk handler, perhaps dual ported, with error checking and typical disk utilities.
- ° Tape playback and decommutator management software including error control.
- ° Data formatter for decommutator bit stream before disk handler.
- ° Electrostatic plotter and display terminal software and or conversion software.

- ° CPU processor to processor communications software.
- ° Executing software task to task communications.
- ° Optimization of operating system overhead in a tailored application.

Additional software could be required for negotiating data (non-dynamic) gathered from central or mission computer on the aircraft which could be stored on the airborne tape recorder. Software with hardware could even reproduce digital voice in real time for data editing. We realize that these two enhancements are not goals but are technically feasible and beneficial for editing.

The ground data processing system might also store information concerning all test configurations. In addition, programmable read only memory (PROM), cassette tape, or floppy disks could be written by the ground data processing to setup control of the airborne equipment at a remote site with appropriate ground interfaces.

4.19 IMPROVED PLOT RESOLUTION

Current "off the shelf" technology supports high resolution, 200 dots per inch, typically 16 by 16 dot matrix electrostatic plotters with printer capabilities. Thruput is limited by paper speeds ranging from 1.0 to 2.0 inches per second. 1.0 ips is the most common paper speed. Paper plots could most reasonably be produced in 11 inch, 15 inch, 20 inch, 22 inch, or 24 inch roll widths or in 11 inch fan-fold width. Comprehensive Fortran compatible plotter software is provided for most major computer vendors which does not include Raytheon. In general, Raytheon hardware and software plotter support is more difficult and expensive but not impossible.

Options are available for the following areas:

- ° Scientific and engineering character expansion.
- ° Hardcopy optional dual port for graphic from Tektronix 40xx model series.

CRT.

- ° Speed throughput boost from vector to raster converter interface.
- ° Off-line plot capability from 9-track tape.

Programmable roll paper cutter was only found for an 11 inch plotter in a 19 inch rack mount. All other paper roll versions have manual cutters.

4.20 DATA EDITING METHODS

4.20.1 ALTERNATE METHODS

Figure 31 represents an evaluation of the magnitude of the editing problem for several of the PCM system operating modes. It was assumed that a large disk (256 megabytes total storage) would be used to store the edited data for processing, and that half the total storage would be available for the edited data with the other half reserved for programs and intermediate storage. The data record length and the disk capacity in number of analysis time series (one time series is the collection of all the required data samples for an analysis of one measurand) are indicated in Table C-17 for extreme and typical values of number of averages and transform size.

Tables C-18 and C-19 summarize important editing considerations as a function of PCM operating mode (for Modes A, B, and C) and playback speed, for 42 track and 28 track recorders, respectively. Decommunication rates include overhead words and only playback speeds resulting in rates higher than 200 kilobits per second are indicated. This is in accordance with recommendations of Reference 21 for playback of randomized NRZ-L coded data.

The analog response is that required for D/A converters and strip chart channels used in editing. The total playback times shown are for 144 measurands at maximum record time. Rewind speed assumed was 240 ips.

The goal of editing is the storage of the selected data time series in a computer compatible form. A minimum of two passes over the recordings will be required to accomplish this - one or more passes (as required) to provide

editing aids to the human editor, and a final pass to perform the selection and storage.

Recorder speed and tape packing density constraints will limit the number of measurands per track to 4-6 for the 20 KHz modes. Therefore, in order to meet the stated goal of editing 12 measurands at a time two or three decommutators would have to be employed.

Editing aids could take one (or more) of the following forms:

- ° Raw time history strip charts obtained from D/A conversion during playback.
- ° Time history plots generated by computer.
- ° RMS, mean, min, max time histories computed and plotted or tabulated.
- ° A crisp summary of candidate time areas and measurands for analysis, provided by a computer, based on user defined criteria - "automatic editing".

4.20.2 AUTOMATIC EDITING

Automatic editing would involve one pass over the data, using an array processor to perform the following functions, then storing the results on disk:

- ° Conversion of data and gain code to array processor floating point format.
- ° Determine minimum and maximum values in each block of N sample values.
- ° Compute the sum of values and sum of squares over each block of N values.

Note only the reduced data (min, max, ΣX , ΣX^2) are saved on disk.

ΣX and ΣX^2 can then be used to compute mean and mean squared and/or variance in each data block. These values from a number of data blocks can then be subjected to a run test (Reference 11) to determine stationarity of the original (source) data. The max and min values can be used to determine the crest factor in each data block - these can be used to evaluate the instrumentation quality.

After a reporting of the instrumentation quality for all channels and candidate stationary regions for analysis to the user, the user selects those time

areas and measurands he wishes to analyze, and the selected data is played back for storage on disk.

For worst case editing involving Mode A data played back at recorded speed (real time) for 12 measurands, only 2 measurands can be automatically edited. Time limitations of the host computer data transfers to and from the array processor and time limitations for array processor calculation thruput are the reasons for this limited responsiveness to recorded speed playback.

Tables C-20 and C-21 show that one measurand may be edited in approximately one half the actual real time of 250 and 500 milliseconds, respectively, for 16,384 and 32,768 total number of 16 bit transfers. This data in both figures was theoretically calculated with an actual measured transfer time factor added in for both a minicomputer (PDP 11/34A) and a super minicomputer (VAX 11/780). The array processor used was a Floating Point Systems AP120B. Thus, only two measurands could be automatically edited at recorded speed playback. If the playback speed was reduced from recorded speed, more measurands could be automatically edited. This would increase edit time.

4.21 MERGING OF ANALYSES FROM MULTIPLE FILTER DATA

The general procedure for this is as follows:

- ° Compute FFT's of data blocks from each filter, separately.
- ° Discard aliased portion of FFT's, as usual.
- ° Discard redundant low frequency results from all but the lowest filter.
- ° Average results as appropriate.
- ° Apply frequency scale.

Figures C-15 and C-16 indicate the record length required to achieve a given number of averages for Modes B and C, respectively. Note that Mode B which has a compression ratio of 227.5 requires longer record lengths to achieve the same number of averages as Mode C which has a compression ratio of only 68.2.

Table C-22 indicates the frequency resolution available with multiple filter modes as a function of the number of samples per filter.

4.22 ADDITION OF ZOOM TRANSFORM AND MODAL ANALYSIS

AFWAL/FIBG currently has modal analysis in one of their mobile vans (Time Data System), and zoom transform and modal analysis in their Sonic Fatigue facility (HP5451B system). One of the goals is to have these capabilities in the Data Analysis area as well. Alternate solutions to this problem are:

- ° Develop application software for the Data Analysis computer system.
- ° Purchase or negotiate the transporting of software already available in the HP and/or Time Data System.
- ° Purchase a new Fourier analysis system featuring modal analysis and zoom transform capability for the Data Analysis area. Such a system would be required to interface with the selected decommutator.

At this time, the latter choice appears to be the best.

5. CONTINUATION OF LITERATURE SEARCH

Literature search activities during Phase II were primarily vendor contacts to determine the current and near-term-future capabilities of PC.1 related equipment. Information was obtained from each of the vendors listed:

ANALOG FILTERS

Frequency Devices, Inc., Analogic, Reticon

TAPE RECORDERS

Honeywell, Bell & Howell, Ampex, Sangamo, Spin Physics

PCM DECOMMUTATION HARDWARE

EMR, DSI

MINICOMPUTER SYSTEMS

Raytheon, Tandem, Digital Equipment Corporation, Hewlett Packard

ARRAY PROCESSORS

Analogic, Floating Point Systems

MODAL ANALYSIS SYSTEMS & SOFTWARE

Structural Dynamics Research Corp., Spectral Dynamics, Hewlett Packard,
Gen Rad (Time Data Division)

PLOTTERS

Versatec, Varian

GRAPHICS TERMINALS

Tektronix

6. FORMULATION OF PCM SYSTEMS

6.1 AIRBORNE PCM ENCODER/FORMATTER

Two basic system architectures are described in this section. The first is a Distributed PCM System and the second is a Centralized PCM System. The two systems utilize many identical subsystems; however, there are significant differences between the systems, as will be shown. Conclusions are given in this section on design tradeoffs which better define the preferred designs in areas such as signal conditioning, filtering, and analog-to-digital conversion. Either definite choices are made or the number of choices to be studied further has been greatly reduced.

A block diagram of the Distributed PCM System is given in Figure C-17. The top half of the figure shows data channels of a Distributed PCM System. The lower half of the figure is the data formatter and digital filter. This part of the system is centrally located and distributed data channels feed data to it through the main data and control bus. The Data Channel and Data Formatter designs are discussed in the following paragraphs. The block diagram shows two data channels multiplexed into one analog-to-digital converter. This is one of the two A/D configurations still under consideration. The other configuration is a dedicated A/D per data channel.

A block diagram of the Centralized PCM System is given in Figure C-18. In the centralized system, the Data Channels and Data Formatter are collocated with cables running out to the 144 remotely located sensors. The top half of the figure shows two data channels. The lower half of the figure is the data formatter and digital filter subsystem. Bus transceivers, buffer storage, and separate control circuits are not required in the centralized system. The Data Channel Interface is different in the centralized system. These

differences are discussed in a later section on the Data Formatter.

6.2 DATA CHANNEL

6.2.1 SIGNAL CONDITIONING - A block diagram of an AGR amplifier is shown in Figure C-19. The system contains a programmable gain amplifier with its associated control circuitry for gain changing and storage. One problem with an auto ranging amplifier is that during gain ranging, transients are introduced to the following stages. This could have adverse effects on system accuracy, unless gain ranging is synchronized with the system. Another alternate is to use a zero crossing detector and only change the gain settings at zero. Gain changing is determined by a peak detector and window comparator. The comparator will have a large hysteresis such that gain steps will not cause oscillation from up to down. The window comparator drives an up/down counter which controls the programmable gain amplifier. The counter output also provides the AGR gain settings to the formatter.

It is estimated that the signal conditioning amplifiers will require 1152 square inches of board area. The power consumption is estimated to be 75 watts.

6.2.2 FILTERING - A basic block diagram of a candidate filtering subsystems is given in Figure C-20. The design utilizes four analog lowpass filters and two digital filters in each of the 144 data channels. It was shown in Section 4.2 that the anti-aliasing filters should be 7-pole Chebyshev filters if VCVS analog filters are used. If switched capacitor filters are used the filters will be the Elliptic type. The Reticon switched capacitor filter R5609 is a 7-pole, 6-zero elliptic lowpass filter. A sampling rate of 3.2768 samples per data cycle is used to give a 66 dB or more alias rejection when either filter is used.

Digital filtering is used for the two lowest frequency filters. The digital filter is the System G digital filter implementation described in Section 4.3. A single high speed multiplier is time shared to perform 78.1 Hz and 19.5 Hz lowpass filtering of the 144 data channels. The digital filter subsystem is centrally located and the analog filters, multiplexers, and analog-to-digital converters may be at distributed locations if desired.

In the Transient Mode, the Four Channel Multiplexers are switched to select inputs from the 20 KHz lowpass filters. Two different data channels are sequentially switched into the high speed A to D converter. All channels are sampled 65,536 times per second. In the Stationary Mode the four analog filters are sequentially sampled and, with the 312.5 Hz filter selected, additional samples are processed in the digital filter circuit. This candidate filtering system, shown in Figure C-20, represents the best preliminary design when size, power required, and performance were considered. The use of digital filters for the two lowest frequency filters offers definite power and size advantages. The following table gives a power consumption and size comparison of VCVS, switched capacitor, and digital filters. The table gives estimated DC power supply input power to operate 144 lowpass filters with a 78.1 Hz cutoff frequency and 144 lowpass filters with a 19.5 Hz cutoff frequency. The VCVS numbers were calculated using size and power numbers given in Table C-5. The switched-capacitor (SC) numbers are based on use of a Reticon R5609, which is an 8-pin integrated circuit, with a capacitor and two resistors for output offset adjustment. A single SC filter was estimated to require 0.75 square inches of board area and require 220 milliwatts of DC power. The digital DC power and size estimates were taken from Tables C-10 and C-11, respectively. The digital (G system) power and size estimates are well below even the switched capacitors estimates. Even if the

digital filter estimates prove to be 10 or 20% low, use of two low frequency digital filters will be justified. Higher frequency digital filters probably should not be used because of the large increase in power consumption, high multiplication rate, and high speed memory required.

POWER CONSUMPTION AND SIZE OF TWO SETS OF 144 FILTERS AT 78.1 Hz AND 19.5 Hz

<u>Filter Type</u>	<u>VCVS</u>	<u>SC</u>	<u>Digital (G System)</u>
DC Power Consumption (Watts)	77.8	63.4	17 to 21
Size (Square Inches)	1037	216	68 to 84

The above table also shows the power and size advantages of using switched-capacitor filters over voltage controlled voltage source filters. As was stated in Section 4.3, the Reticon switched-capacitor filter is an unproven device at this time but seems to have good potential for this application. Performance over a wide temperature range may be a significant problem area. Power consumption of the Reticon filter is higher than desired. If filter settling time will permit, it may be possible to replace the four lowpass filters with one or two variable frequency lowpass filters. Cutoff frequency of switched capacitor filters can be tuned by changing the switching frequency supplied to the filter.

Total size estimate for the filters in a 144 channel system is 516 square inches of printed circuit board area. Total power consumption is 148 watts. These estimates are for the system shown in Figure C-20 with four Reticon filters and two digital filters per channel.

6.2.3 ANALOG TO DIGITAL CONVERSION - One of the first tasks in defining the system architecture is selection of the type of ADC to be used. The possible ADC candidates are the successive approximation and parallel encoding with sub-ranging.

The successive approximation has advantages in all aspects except encoding time. In a multiplexed configuration the mux, input S/H settling times, and amplifier settling times dictate the maximum sampling rate or the number of multiplexer channels.

The typical settling time for a multiplexed configuration is approximately 4-5 microseconds. This would produce at best a mux capability of three at the highest sampling rate with parallel encoding. The successive approximation ADC could be multiplexed two times. This does not provide for much of a system improvement with the parallel encoder, especially when its power consumption is considered. It now becomes a pretty clear cut choice to select the successive approximation ADC over the parallel encoder.

With the number of multiplexed channels being limited to two, is it worth the addition in system complexity to multiplex channels, or is it better to have a dedicated ADC for each channel? The latter would provide output data for all channels simultaneously to the data latches and would eliminate the inherent timing problems of multiplexed data. This leads to two possible ADC candidates for study in the next phase. The dedicated ADC is shown in Figure C-21 and the multiplexed configuration in Figure C-22. Both systems require the use of sample and hold circuits to reduce the aperture time and provide the required simultaneous sampling. Output data latches are provided to allow the formatter to operate one word behind.

The total size estimates for the dedicated system is 676 square inches and 516 square inches for a two level mux configuration. The total power estimate is 370 watts for the dedicated system versus 231 for the two level multiplexed configuration. The power estimates include the use of monolithic S/H circuits and the output latches.

6.3 DATA FORMATTER

The PCM system data formatter supplies timing and control information to three interfaces; data channel sampling and control, data buffer memory addressing and control, and PCM formatting to the tape recorder interface. The timing and control signals for each of the sampling modes are derived from parameters stored in a programmable format memory by the format controller microprocessor. The block diagram for the data formatter is shown in Figure C-23.

6.3.1 Data Channel Interface

The data formatter supplies channel select and filter select codes, calibration and gain change enable signals, and the sample rate clock to the data channel interface. The digitized data and gain codes are transferred either directly to the tape recorder interface for transient data sampling, or to the data buffer memory for stationary data sampling modes. .

At a sample rate of 65,536 samples per second, the data channel interface receives 15 bit data words from up to 144 channels in a 15.25 microsecond period. For a centralized configuration of the PCM system, a buffer register is required for each channel to store the results of the previous A/D conversion for multiplexing into the data buffer memory or tape recorder interface. The multiplexer is configured as two banks of 4 to 1 multiplexers. The first bank outputs 36 data tracks with four measurands per track for transient data recording. The second multiplexer bank outputs 9 data tracks with 16 measurands per track to the data buffer memory for stationary data recording modes. The centralized configuration supplies control signals common to all data channels. These include the sample rate clock, filter select codes, and calibration and gain change enable signals. The block diagram for the data channel interface for a centralized PCM system is shown in Figure C-24.

Distributed PCM systems require central unit/remote unit interfaces to implement the data channel select and control functions. Serial and parallel interfaces, as discussed in Section 4.14, are realizable for the data sampling goals of the PCM system. Either approach requires multi-channel data buffers in the remote units to store sampled data for acquisition by the central unit during each sample period. Interface hardware and timing requirements, and versatility in the channel capacity configurations of the remote units, are more readily implemented with a parallel, full-duplex, command/response interface.

Timing requirements include the system goal for a maximum interchannel sampling phase error of $\pm 5^\circ$ at 10 KHz. Phase errors are determined primarily by the analog components in the data channels and sample clock jitter. For distributed systems, additional phase errors are introduced by sample clock coherency between remote units due to cabling propagation delays, interface signal rise and fall times, and synchronization jitter between central unit transmission and remote unit detection of the sample commands. Analog component phase errors can be compensated for by pre-flight calibration techniques. Sample clock jitter can be minimized to values in the range of 10 to 20 nanoseconds by careful design techniques.

Distributed system phase errors due to central unit/remote unit synchronization may be alleviated by configuring the interface with an additional line for a clock signal to minimize the sample command synchronization jitter. Cable propagation delays between the central unit and remote units contribute the major component for phase errors due to system timing signals. Equal length cables are impractical for most applications. A pre-flight calibration technique with a known signal applied to at least one channel of each remote unit will supply compensation data for cable propagation delays.

A distributed PCM system requires additional hardware to implement the command/response data acquisition bus. The bus format contains command words to address the remote units with each command word followed by a number of data word replies equal to the channel capacity of the remote unit. Data buffers are required in the remote units to store the digitized data from the previous sample period. A FIFO buffer is required in the central unit to synchronize the data replies. Received data is demultiplexed to 9-track data for buffer memory storage in stationary data sampling modes, and to 36-track data to the tape recorder interface for transient data sampling. The block diagram for the data channel interface for a distributed PCM system is shown in Figure C-25.

6.3.2 DATA BUFFER MEMORY - The data buffer memory is required for stationary data sampling modes to accumulate high sample rate data while transmitting multi-track formatted data to the tape recorder. Ideally, the memory would be implemented with FIFO memory devices to minimize memory control logic. However, with the large amount of data word storage required, available FIFO devices would require an unreasonable amount of power and P.C. board area. Large capacity dynamic RAM's with read and write address counters meet the storage requirements as defined in Section 2.4.2

The maximum configuration for 2048 samples per filter, and sampling 6 filters, requires 270 memory I.C.'s, with a capacity of 64K bits per device. The peak power required is approximately 19 watts, with an average power of 4 watts. P.C. board area is approximately 135 in.².

The memory is configured in nine segments to reduce the memory cycle time required for each segment. Memory devices with cycle times of 250 nsec allow

ample time for read, write, and refresh cycles at the highest channel sample rate. Each of the nine memory segments is organized as 128K words by 15 bits per word. A 16 word FIFO buffer is utilized for data storage and synchronization at the input of each segment. The memory outputs are demultiplexed for 9 or 36 track data to the tape recorder interface. The block diagram for the data buffer memory is shown in Figure C-26.

6.3.3 Format Controller

The format controller is implemented with high speed bit-slice processors and microprogram controllers from the 2900 family of devices. Data sampling and PCM format parameters are stored in a format control memory programmable by external ground equipment.

Data sampling parameters include both calibration and in-flight sampling formats. The sampling parameters include the number of filters sampled, range of the filter index numbers, the number of samples per filter, and the number of channels sampled.

PCM format parameters include the number of words per frame, the frame synchronization patterns, and the number of recorder tracks utilized.

The format controller microprocessor derives the sampling and PCM formats from the stored parameters and from various interface status signals and selects the applicable routines and subroutines stored in the microprogram memory. This memory is implemented with fusible-link high speed bipolar PROM's. The microprogramming capability of the controller processor provides for future changes to the system architecture and formatting capabilities by changes of the microprogram.

The format controller requires approximately 60 square inches of P.C. board area and 16 watts of power.

6.4 ANALYSIS, EDIT, AND DISPLAY SYSTEMS

Ground data processing systems consist of two candidates for editing, analysing, and displaying data played back from the airborne tape. The first less costly "basic" candidate meets the same required goals as the second candidate but at the price of overall throughput. Neither candidate can produce with a single electrostatic plotter one half plot per second at an 8 1/2" by 11" plot size, a required goal. Of course two plotters could fulfill this goal. The "high capacity" candidate has more throughput potential because it utilizes three decommutators concurrently at approximately 4.9 megabits per second (Mb/S) each giving 1.83 megabytes per second (MB/S) total input. Both these candidates appear in Figures 27 and 28.

The basic candidate utilizes three decommutators concurrently at approximately 1.44 Mb/S each or .54 MB/S total input. Editing is accomplished with two six-channel visicorders. The visicorder shown has limited frequency response past 5 KHz. This requires a reduction in playback speed by a factor of four from the recorded speed for Mode A. However, most other modes permit and some even require playback increases to conform to IRIG standards.

The single bus represented has limited bandwidth, so .54 MB/S input and the same for disk output results in a 1.08 MB/S total bus rate. The single bus of today's typical minicomputer cannot be expected to continuously operate at any higher rates. 4.2 megabytes disk storage is the minimum requirement to store one single 16-second data interval for 2 measurands from Mode A. As previously mentioned under Section 4.20, Data Editing Methods, automatic editing is feasible for two measurands played back at some reduced speed due to single bus bandwidth limitations.

The basic candidate has the following attributes:

- ° Single bus typically quoted in advertisements from 1.2 MB/S to 2.7 MB/S transfer rates.
- ° System disk with operating system and applications code using standard, unmodified disk handler software and logical file structure.
- ° Disk dedicated to airborne data. This disk may have a modified software disk handler and/or modified logical file structure to optimally handle the volume of airborne data efficiently.
- ° Tape unit for system generations and possible disk file backups and restores.
- ° Procured or developed decommutator interface for multiplexing three bit streams into a Direct Memory Access (DMA) bus transfer request.
- ° Array processor for analysis and display.
- ° 256 K bytes maximum memory on minicomputer.
- ° 12 channel word selector with DACs to accommodate two 6-channel visicorders.
- ° Electrostatic plotter with 200 dots/inch resolution.
- ° Tektronix 4012 CRT as console and/or graphics display terminal.
- ° Highspeed line printer, possibly 11" Gould electrostatic plotter with the proper interface hardware.

The high capacity candidate can radically depart from visicorder editing which is supported as an option shown by the dotted lines in Figure C-28. As previously mentioned under Section 4.20, Data Editing Methods, automatic editing is feasible for two measurands played back at recorded speed. It is possible that a higher number of measurands could be automatically edited with some fine tuning of the software within the array processor and super minicomputer.

The high speed master bus is typically quoted in advertisements from 13 to 26 MB/S. Both medium and high speed buses dedicated to a device may be configured on the high speed master bus. Multiple disks with dedicated controllers enable the 1.83 MB/S coming as input to go to disk at an equivalent output rate.

Throughput efficiency requires a dedicated disk path per decommutator. The system disk, tape unit, decommutator interface, 12 channel word selector with DACs, 6 channel visi orders, electrostatic plotter, Tektronix 4012 CRT, and high speed line printer remain configured for the same reasons as in the basic candidate system.

The array processor is shown with a high capacity input and output interface which requires a procured or developed bus converter. Unlike the basic candidate, the array processor has a higher throughput potential because of this high speed interface.

Either the basic or high capacity candidates could support all AFWAL/FIBG required analysis goals if applicable software was implemented or procured. Even though a significant amount of current software has been implemented in Fortran, and thus, may be portable to another computer, it may not be feasible in view of the scope of the acquisition system.

In summary, the following table outlines attributes for both the basic and high capacity candidate systems:

GOAL	BASIC CANDIDATE	HIGH CAPACITY CANDIDATE
ENCODING RESOLUTION	YES	YES
MAXIMUM ARRAY SIZE 16,384 16 BIT WORDS (INPUT)	YES	YES
COMPUTER PRECISION 32 BITS FLOATING POINT	YES	YES
EDIT CAPABILITY 12 CHANNELS	YES	YES
THRUPUT (SINGLE PLOTTER) .5 8 1/2" X 11" PLOTS/SEC (MULTIPLE PLOTTERS)	NO YES	NO YES
RESOLUTION 160 DOTS/INCH	YES	YES
FORTRAN CALLABLE PLOT SOFTWARE	YES	YES
ANALYSIS SOFTWARE	YES	YES

7. RECOMMENDATIONS

The evaluation of the results of Phase II have shown that the airborne tape and ground systems may be considered mutually independent of each other with respect only to their applicable goals.

7.1 AIRBORNE ENCODER/FORMATTER SYSTEM

The eight candidate configurations each possess the capability of fulfilling the primary system goals defined in Phase I. The goals for physical characteristics (power, weight and size) were not achieved and are recommended for trade-off study in Phase III. These candidates have three levels of design consideration:

- a) Distributed versus centralized architecture
- b) Filter type - Voltage Controlled Voltage Source analog versus switched capacitor filters
- c) Dedicated versus multiplexed ADC implementation

MCAIR recommends evaluation of the three choices above be made mutually independent of each other during Phase III. System characteristics given in Section 2., Table C-2, based on the multiple lowpass encoding scheme will remain unchanged during Phase III.

Power, weight, and size are impacted as follows by the three choices:

<u>Distributed vs. Centralized</u>	
Power	Approx. 12% higher with distributed
Weight	Approx. 38% heavier with distributed
Volume	Approx. 34% higher with distributed
<u>VCVS vs. SCF</u>	
Power	233 more watts using VCVS
Weight	No appreciable impact
Volume	No appreciable impact
<u>Dedicated A/D versus MUX'ed A/D</u>	
Power	48 more watts using dedicated A/D
Weight	No appreciable impact
Volume	No appreciable impact

The choice of architecture (distributed versus centralized) has a potential impact on the following standards: maintainability, modularity, test readiness, operational flexibility, recurring manpower support, and hardware cost as well as power, weight and size. A trade-off study is recommended which embraces all of these standards. Further, a detailed survey of AFWAL/FIBG historical tests must be performed for:

- o number of tests performed concurrently,
- o number of measurands for each test, and
- o frequency response required per test.

These results will be employed in the study to evaluate and provide recommendations to AFWAL/FIBG as to the values of a distributed and centralized type of system.

The choice of filter types has a potential impact in accuracy, inter-channel phase error, dynamic range plus hardware cost and power. Trade-off study in these areas is recommended. Also, a study of calibration method with respect to filter specifications is recommended.

The choice of A/D implementation has a potential impact on accuracy, maintainability, hardware cost, and power. Trade-off study in these areas is recommended.

With completion of these studies, the three basic design levels of the airborne acquisition system may be resolved.

7.2 RECORDER/REPRODUCER SYSTEM

One possible choice here is between a 28-track and 42-track head configuration. Using a 28 track recorder, the proposed IRIG 106-80 recommendation on bit packing density will be exceeded slightly for Modes A and C. However, a significant saving in tape recorder size, weight and power is possible. Trade-off

studies of Phase III should include the 28-track versus 42-track consideration, as well as a study of one versus two recorders.

7.3 GROUND ANALYSIS, EDIT AND DISPLAY SUBSYSTEM

The two ground configurations presented both fulfill the required goals. It is to be noted that numerous potential configurations exist that lie between those presented. In order to **assess** the most appropriate system for AFWAL/FIBG a **trade-off** study is recommended which evaluates the system throughput potential versus recurring manpower cost. Additionally, survey must be performed to **assess** historical tests for test hours recorded per project to determine a reasonable throughput requirement to avoid significant processing backlog.

7.4 CONTINUATION OF STUDY

Based on the results of Phase II as presented herein, MCAIR recommends approval of Phase II and initiation of Phase III, Evaluation of PCM Systems.

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FIGURES AND TABLES

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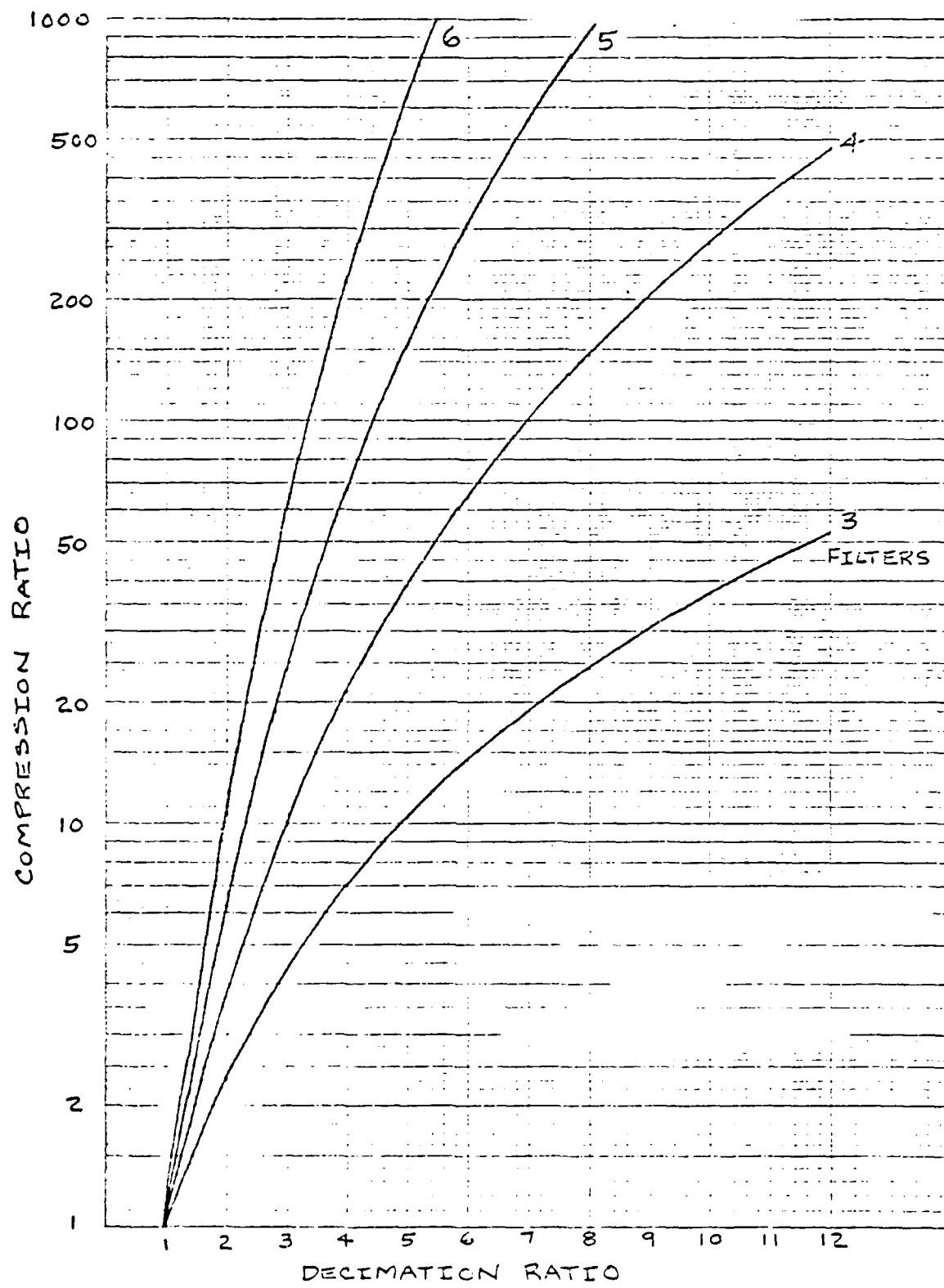


FIGURE C-2
MULTIPLE FILTER ENCODING SAMPLE RATE COMPRESSION
VERSUS DECIMATION RATIO

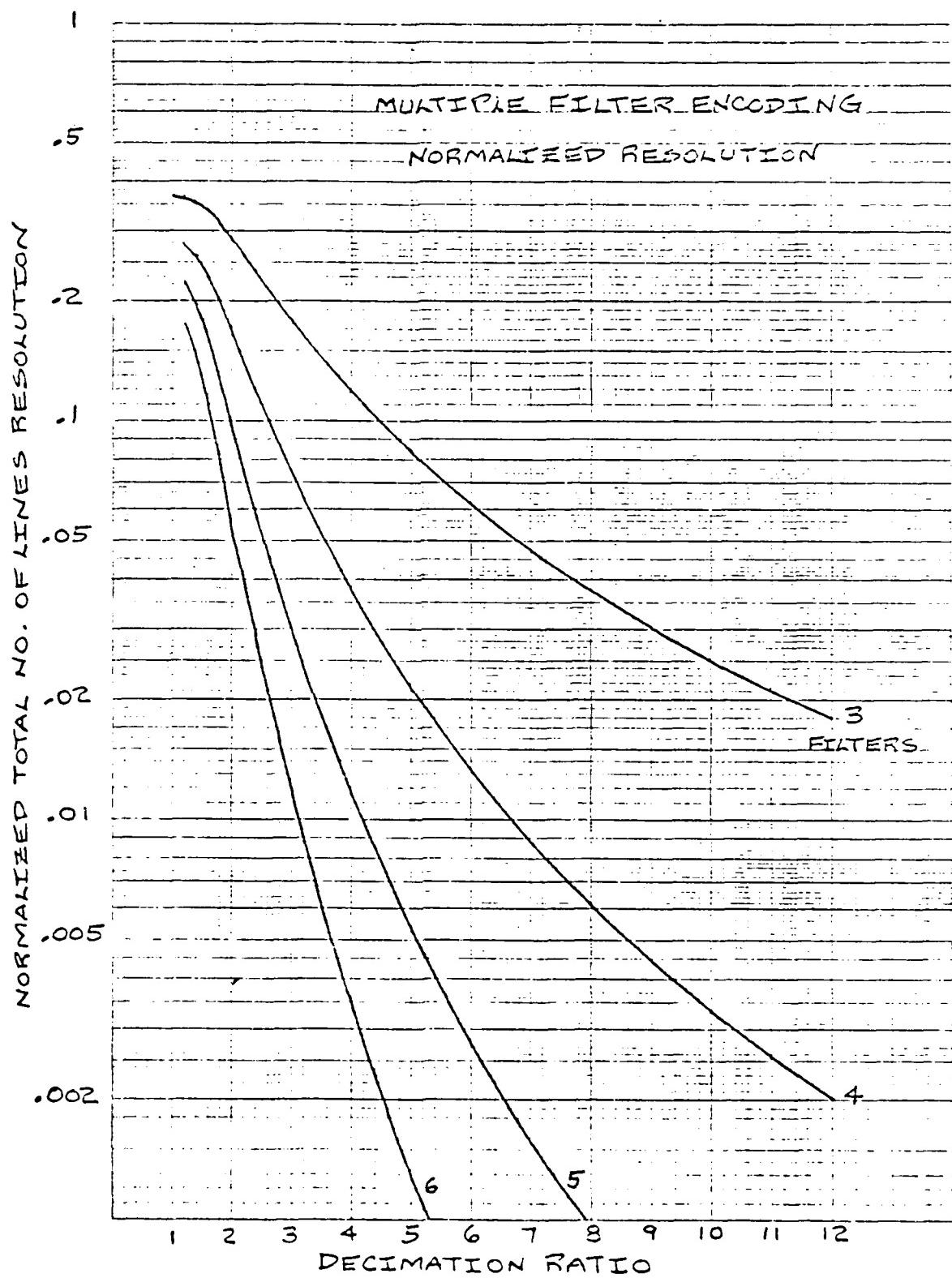


FIGURE C-3

TABLE C-1
ALTERNATE MULTIPLE FILTER CONFIGURATIONS

<u>Configuration Designation</u>	<u>No. of Filters Per Measurand</u>	<u>Cutoff Frequency Separation</u>
1A	4	1 decade
2A	4	3 octaves
3A	6	2 octaves
4A	8	.5 decade
5A	12	1 octave

TABLE C-2
MULTIPLE FILTER ENCODING CONFIGURATION 3A (REVISED 18 MAY 80)
CUTOFF FREQUENCY SEPARATION 2 OCTAVES (DECIMATION RATIO = 4)

FILTER NO.	CUTOFF FREQUENCY (Hz)	WORST-CASE RANGES			
		SAMPLES/CYCLE	BITS/SAMPLE	2.5 to 4.1	12 to 16
0	20000	-	-	-	-
1	5000	-	-	-	-
2	1250	-	-	-	-
3	312.5	-	-	-	-
4	78.125	-	-	-	-
5	19.53125	-	-	-	-
ROUTE (# FILTERS SAMPLED)	ANALYSIS RANGE (Hz)	TOTAL NO. OF LINES RESOLUTION	TIME UPDATE (SECONDS)	SAMPLES PER FILTER PER UPDATE	BUFFER STORAGE (WORDS PER CHANNEL)
B 0 - 5	0 - 20000	74 - 121 593 - 972 2312 - 3691	1.07 - 1.75 8.52 - 13.98 34.09 - 55.91	64 512 2048	233 1857 7427
C 0 - 4	0 - 20000	62 - 102 499 - 819 1993 - 3276	0.266 - 0.437 2.13 - 3.49 8.52 - 13.97	64 512 2048	177 1410 5640
E 1 - 5	0 - 5000	62 - 102 499 - 819 1993 - 3276	1.06 - 1.75 8.52 - 13.98 34.07 - 55.87	64 512 2048	177 1410 5640
F 1 - 4	0 - 5000	50 - 83 405 - 665 1623 - 2662	0.265 - 0.435 2.12 - 3.48 8.49 - 13.93	64 512 2048	129 1031 4121
H 2 - 5	0 - 1250	50 - 83 405 - 665 1623 - 2662	1.06 - 1.74 8.49 - 13.93 33.97 - 55.71	64 512 2048	126 1031 4121
I 2 - 4	0 - 1250	39 - 64 312 - 512 1248 - 2048	0.262 - 0.430 2.10 - 3.44 8.39 - 13.76	64 512 2048	83 659 2634
A 0	0 - 20000	-	-	-	600,000
D 1	0 - 5000	-	-	-	150,000
G 2	0 - 1250	-	-	-	17,500
J 3	0 - 312.5	-	-	-	5,375
K 4	0 - 78.1	-	-	-	1,975
L 5	0 - 19.5	-	-	-	744

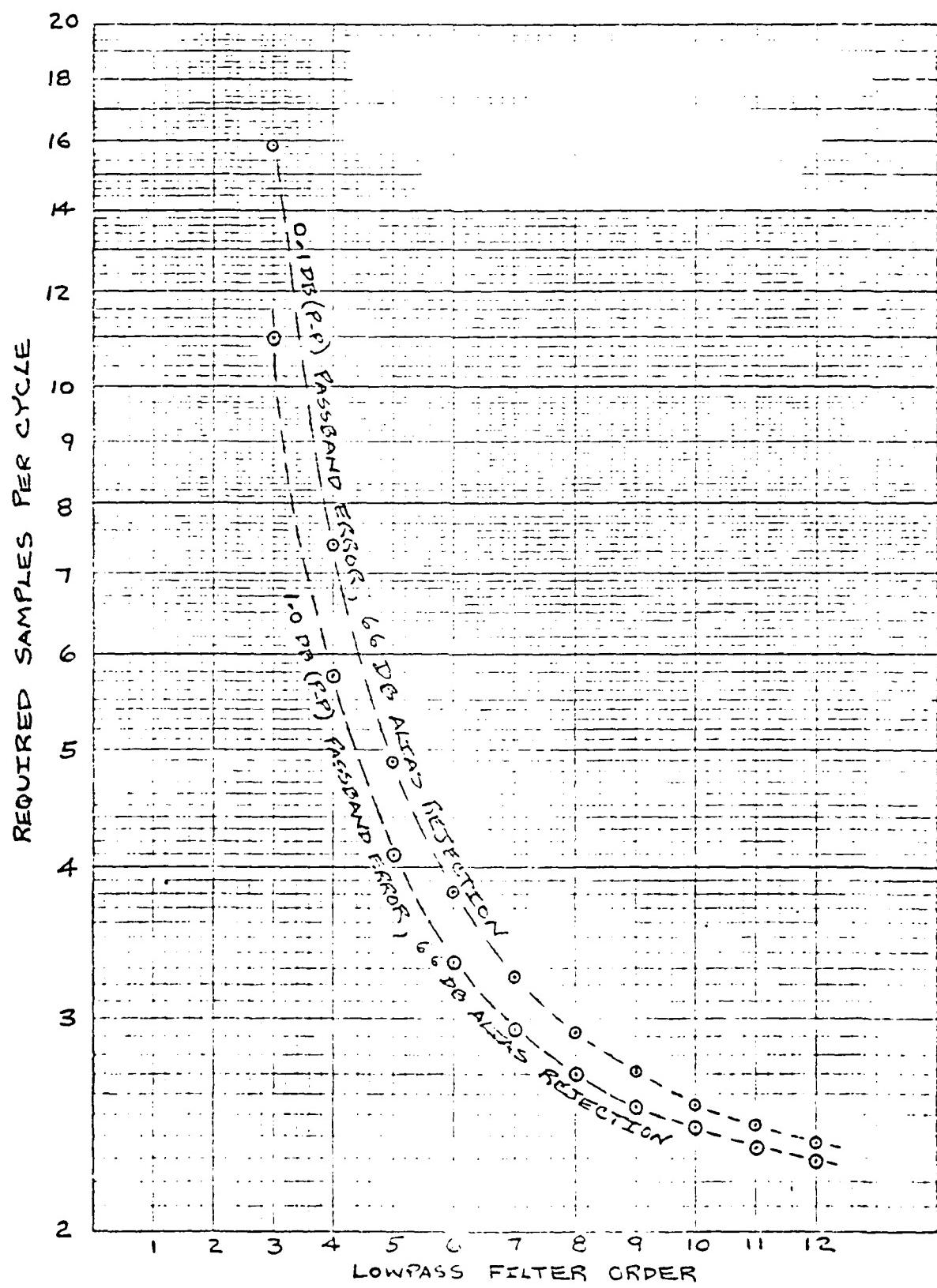


FIGURE C-4

REQUIRED SAMPLES PER CYCLE VERSUS ANTI-ALIAS FILTER ORDER (CHEBYSHEV FILTERS)

TABLE C-3

ANTI-ALIAS FILTER CHARACTERISTICS

	<u>5 Pole</u>	<u>6 Pole</u>	<u>7 Pole</u>	<u>8 Pole</u>
• Size	1.4 sq in	1.8 sq in	2.0 sq in	2.4 sq in
• Power	180 mw	270 mw	300 mw	360 mw
• Sampling Rate	82 KHz	67 KHz	59 KHz	54 KHz
• Offset Factor	.75	1	1.1	1.3

TABLE C-4
PCM System Operating Modes

Filter No.	Cutoff Frequency	Sample Rate	Based on 16 bits per sample.	
			Frequency and Time Resolution	Bit Rate for 144 Channels (MEGABITS/SEC)
0	20000 Hz	65536 Hz		
1	5000	16384		
2	1250	4096		
3	312.5	1024		
4	78.125	256		
5	19.3125	64		
* Determined in ground processing			Based on 16 bits per sample.	
Operating Mode Definition	Analysis Frequency Range (Hz)	Total no. of lines	Seconds per Update	
Filters Sampled	No. of samples per filter per update			
B 0-5	64 512 2048	92 742 2968	1.333 10.664 42.656	0.6637 - -
C 0-4	64 512 2048	78 625 2500	0.333 2.664 10.656	2.2140 - -
A 0	*	*	*	150.995 6.79 x 10 ¹⁰ -
E 1-5	64 512 2048	78 625 2500	1.332 10.666 42.625	0.5535 - -
F 1-4	64 512 2048	63 507 2031	0.332 2.656 10.625	1.7764 - -
D 1	*	*	*	37.749 1.70 x 10 ¹⁰ -
H 2-5	64 512 2048	63 507 2031	1.328 10.625 42.5	0.4441 - -
I 2-4	64 512 2048	48 390 1562	0.328 2.625 10.5	1.3482 - -
C 2	*	*	*	9.437 0.425 x 10 ¹⁰ -
J 3	*	*	*	2.359 0.106 x 10 ¹⁰ -
K 4	*	*	*	0.5098 0.0265 x 10 ¹⁰ -
L 5	*	*	*	0.1415 0.00674 x 10 ¹⁰ -

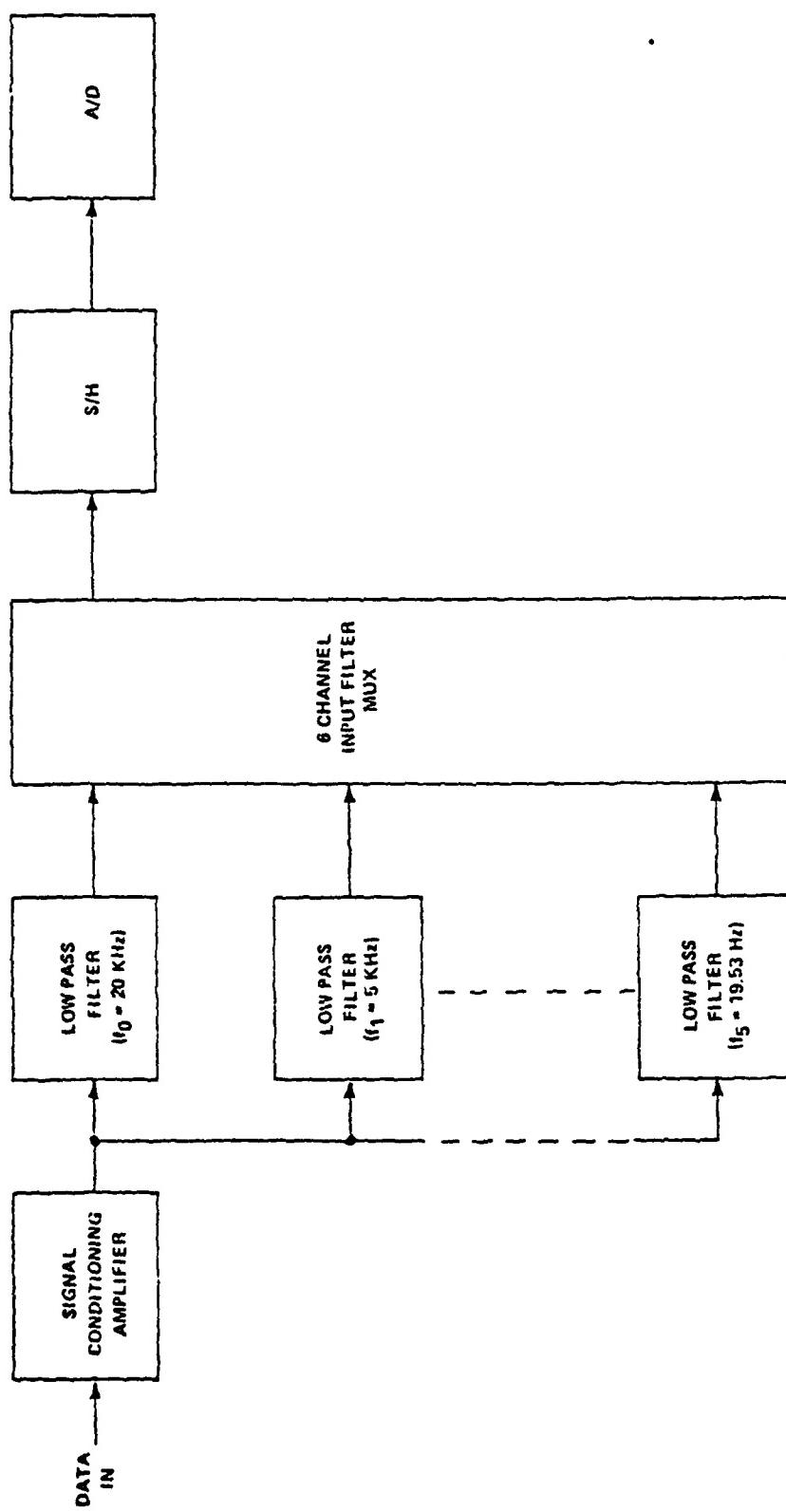


FIGURE C-5
MULTIPLE ANALOG FILTER BLOCK DIAGRAM

TABLE C-5
LOW PASS FILTER CHARACTERISTICS

	<u>5 Pole</u>	<u>6 Pole</u>	<u>7 Pole</u>
• Size (1)	1.4 sq in	1.8 sq in	2.0 sq in
(2)	1.5 sq in	1.9 sq in	2.2 sq in
(3)	3.1 sq in	3.6 sq in	4.6 sq in
• Power	180 mw	270 mw	270 mw
• Offset Factor	.75	1	1.1
	(1) f_0 and f_1 filters		
	(2) f_2 and f_3 filters		
	(3) f_4 and f_5 filters		

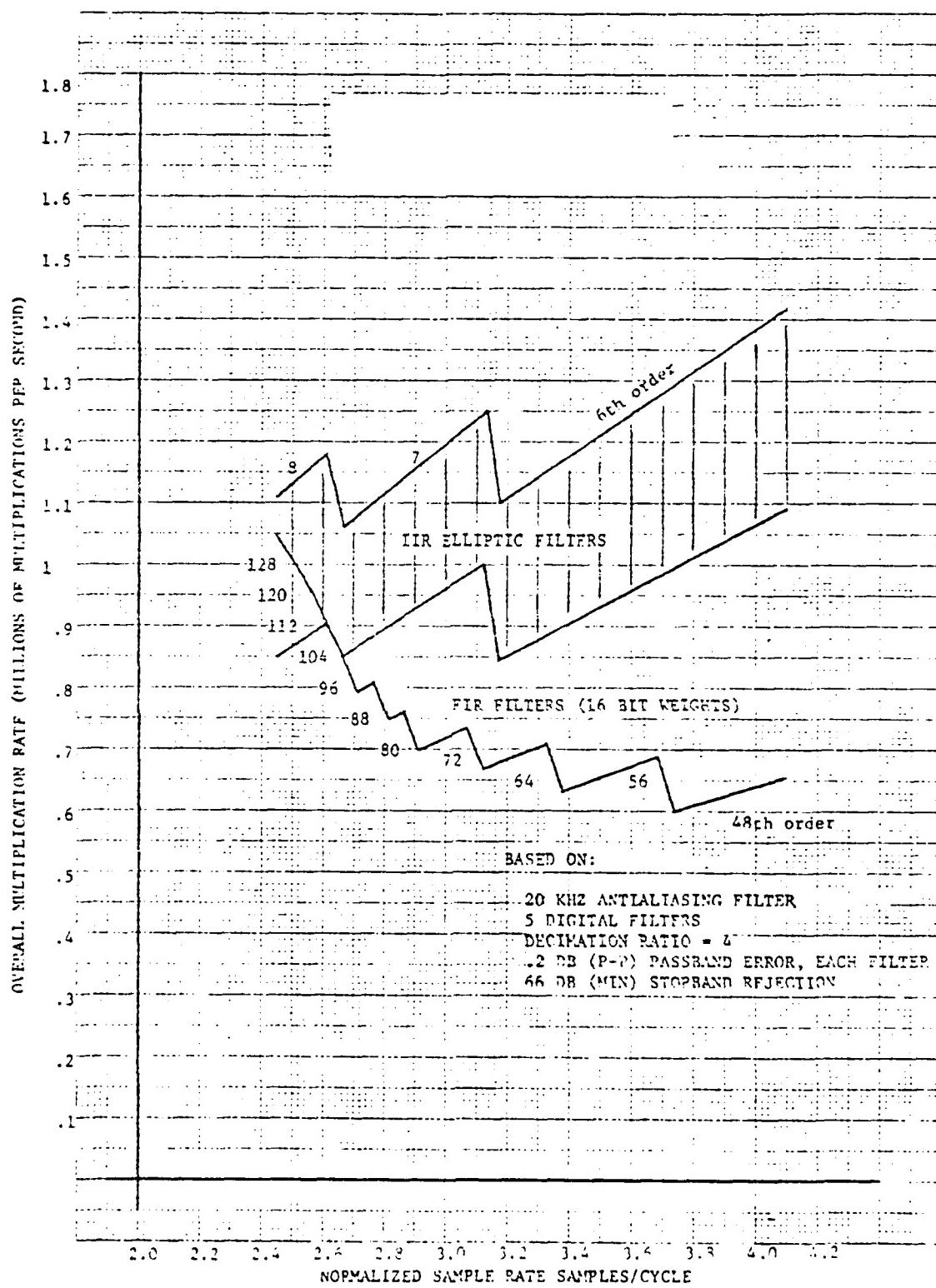


FIGURE C-6

MULTIPLE FILTER ENCODING DIGITAL FILTER IMPLEMENTATION COMPARISON IIR VERSUS FIR FILTERS

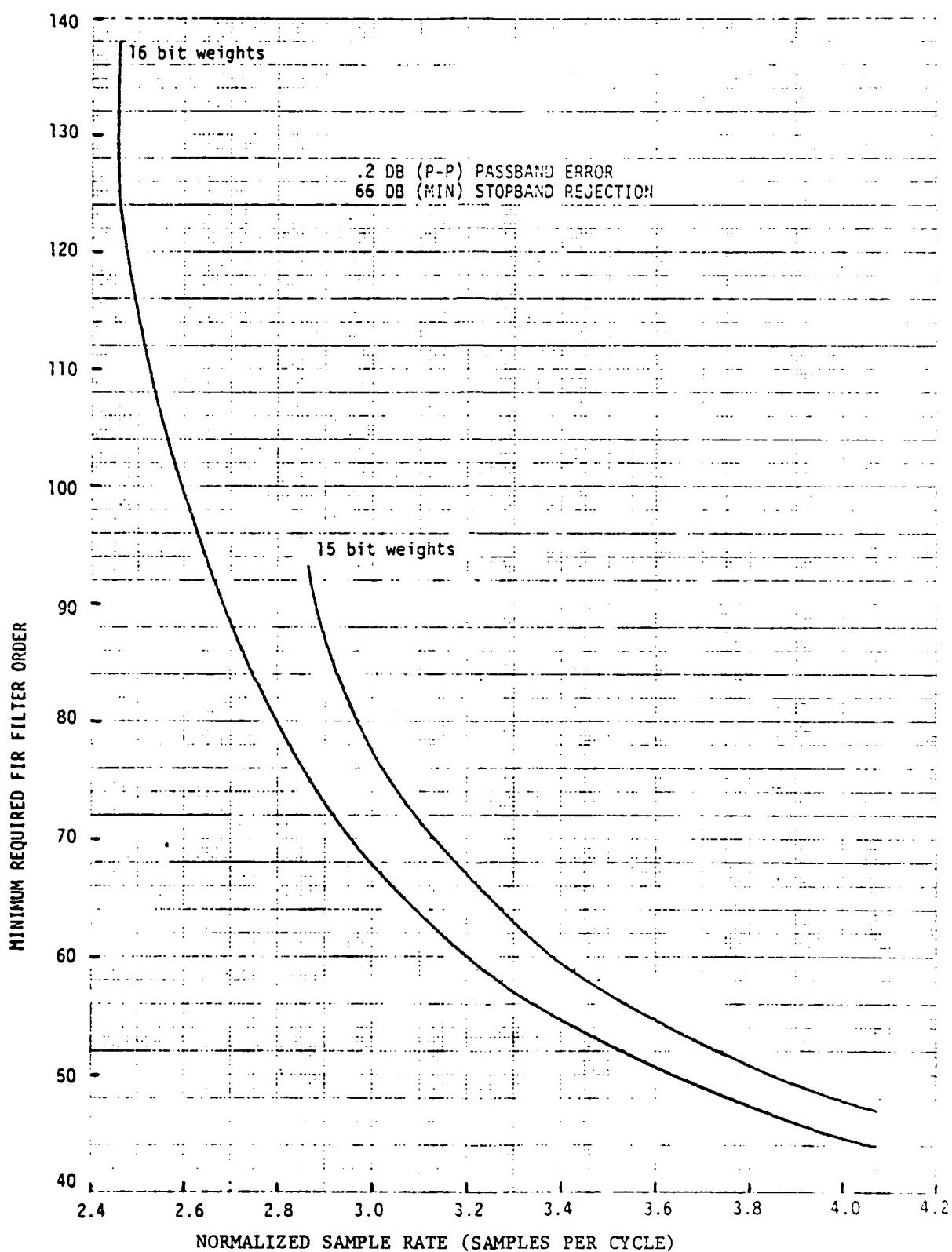


FIGURE C-7
MULTIPLE FILTER ENCODING CONFIGURATION 3A
FIR DIGITAL FILTERS (FILTER ORDER VERSUS SAMPLE RATE)

TABLE C-6

FIR 16T IMPULSE RESPONSE (FIR)
LINEAR PHASE DIGITAL FILTER DESIGN
HIGHPASS FILTER

FILTER LENGTH = 64

	IMPULSE RESPONSE
H1	1.0 -0.305510 -0.3 E H1
H2	-0.734901 J -0.3 E H1
H3	-0.10924001 -0.2 E H1
H4	-0.14755001 -0.2 E H1
H5	-0.73633301 -0.3 E H1
H6	-0.29627301 -0.3 E H1
H7	0.10924001 -0.2 E H1
H8	0.14755001 -0.2 E H1
H9	0.73633301 -0.3 E H1
H10	0.29627301 -0.3 E H1
H11	-0.734901 J -0.3 E H1
H12	-0.10924001 -0.2 E H1
H13	-0.14755001 -0.2 E H1
H14	-0.73633301 -0.3 E H1
H15	-0.29627301 -0.3 E H1
H16	-0.10924001 -0.2 E H1
H17	-0.14755001 -0.2 E H1
H18	-0.734901 J -0.3 E H1
H19	0.10924001 -0.2 E H1
H20	0.14755001 -0.2 E H1
H21	0.73633301 -0.3 E H1
H22	0.29627301 -0.3 E H1
H23	-0.10924001 -0.2 E H1
H24	-0.14755001 -0.2 E H1
H25	-0.734901 J -0.3 E H1
H26	-0.29627301 -0.3 E H1
H27	-0.10924001 -0.2 E H1
H28	-0.14755001 -0.2 E H1
H29	-0.734901 J -0.3 E H1
H30	-0.29627301 -0.3 E H1
H31	-0.10924001 -0.2 E H1
H32	-0.14755001 -0.2 E H1
H33	-0.734901 J -0.3 E H1
H34	-0.29627301 -0.3 E H1
H35	-0.10924001 -0.2 E H1
H36	-0.14755001 -0.2 E H1
H37	-0.734901 J -0.3 E H1
H38	-0.29627301 -0.3 E H1
H39	-0.10924001 -0.2 E H1
H40	-0.14755001 -0.2 E H1
H41	-0.734901 J -0.3 E H1
H42	-0.29627301 -0.3 E H1
H43	-0.10924001 -0.2 E H1
H44	-0.14755001 -0.2 E H1
H45	-0.734901 J -0.3 E H1
H46	-0.29627301 -0.3 E H1
H47	-0.10924001 -0.2 E H1
H48	-0.14755001 -0.2 E H1
H49	-0.734901 J -0.3 E H1
H50	-0.29627301 -0.3 E H1
H51	-0.10924001 -0.2 E H1
H52	-0.14755001 -0.2 E H1
H53	-0.734901 J -0.3 E H1
H54	-0.29627301 -0.3 E H1
H55	-0.10924001 -0.2 E H1
H56	-0.14755001 -0.2 E H1
H57	-0.734901 J -0.3 E H1
H58	-0.29627301 -0.3 E H1
H59	-0.10924001 -0.2 E H1
H60	-0.14755001 -0.2 E H1
H61	-0.734901 J -0.3 E H1
H62	-0.29627301 -0.3 E H1
H63	-0.10924001 -0.2 E H1
H64	-0.14755001 -0.2 E H1

before rounding to 16 bits

$$\sum_1^4 h(n) = 1.0071957 + .0688 \text{ dB}$$

$$\sum_1^4 h^2(n) = \frac{1}{2} 0.362215 = .181107$$

after rounding to 16 bits 2's complement

$$\sum_1^4 h(n) = 1.007812493 + .0676 \text{ dB}$$

$$\sum_1^4 h^2(n) = .0.181097633$$

cumulative DC error (after rounding)

$$\sum_1^4 h(n) = 3.328 \text{ dB}$$

$$\sum_1^4 h^2(n) = .270$$

$$\sum_1^4 h(n) = .203$$

$$\sum_1^4 h^2(n) = .135$$

LOWER BAND EDGE 0.0 HAND 1 (A/D) 2 (A/D) 2 (A/D)

UPPER BAND EDGE 0.074294005 0.125730000

OF CLIPED VALUE 0.500000000 0.500000000

OF LINEAR 1.000000000 1.1555999976

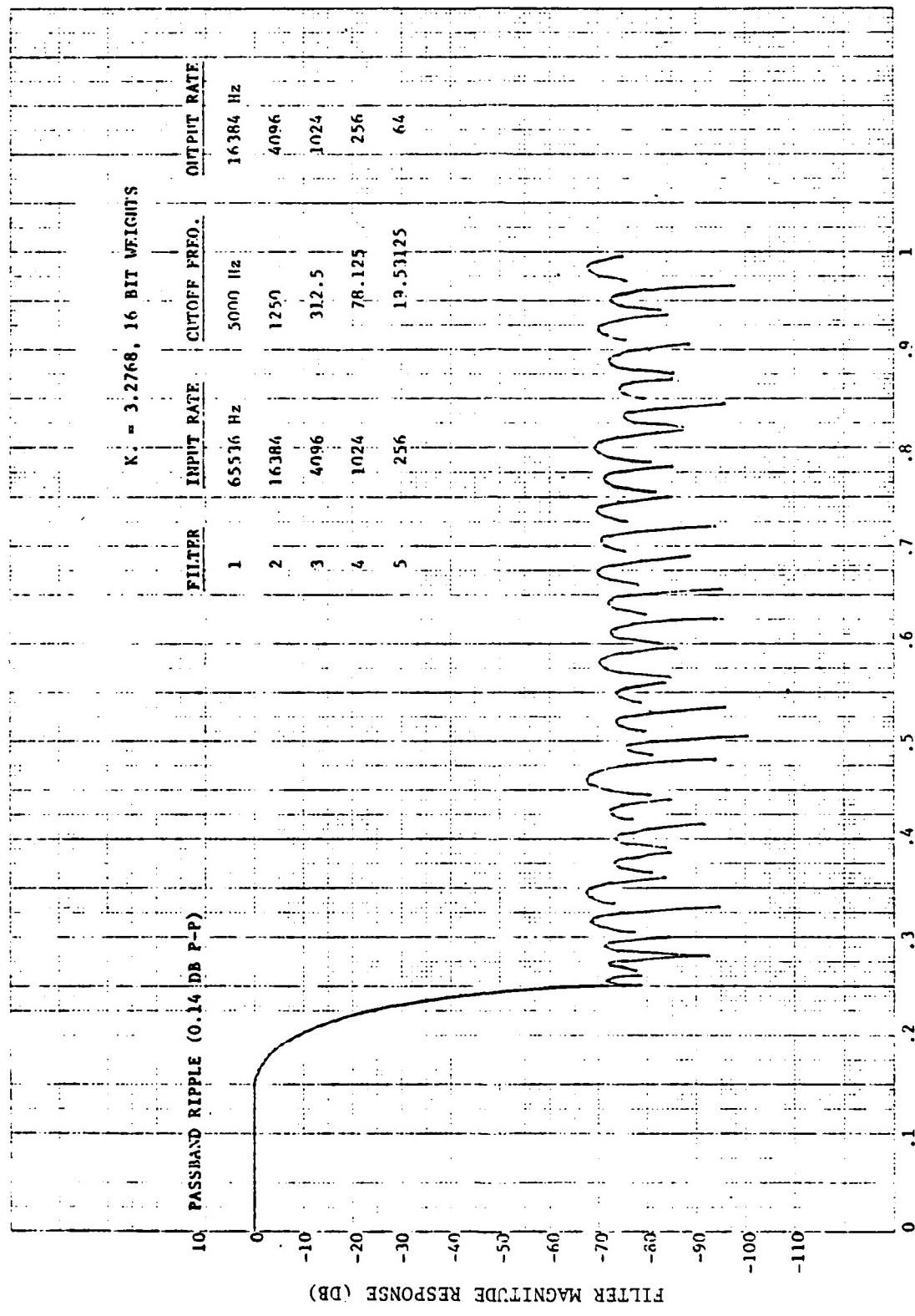
OF VARIOUS 0.000000000 0.000000000

IN VARIOUS 0.000000000 0.000000000

DI VARIOUS 0.000000000 0.000000000

TABLE C-7
 CONFIGURATION 3A FIR DIGITAL FILTER 64 WEIGHTS
 SAMPLE RATE 65536 Hz CUTOFF FREQUENCY 5000 Hz
 FILTER WEIGHTS ROUNDED TO 16 BITS TWO'S COMPLEMENT

WEIGHT INDEX	DECIMAL EQUIVALENT ROUNDED TO 16 BITS	BIT NUMBER 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
C1	-3.9672852E-4	1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1
C2	-7.3242188E-4	1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 0 0
C3	-1.0986328E-3	1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 0 0
C4	-1.1901855E-3	1 1 1 1 1 1 1 1 1 1 1 0 1 1 0 0 1
C5	-7.6293945E-4	1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1
C6	3.0517578E-4	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0
C7	1.8310547E-3	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0
C8	3.4484863E-3	0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 1
C9	4.3945313E-3	0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0
C10	4.0588379E-3	0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 1 0
C11	2.0446777E-3	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1 1
C12	-1.3732910E-3	1 1 1 1 1 1 1 1 1 1 1 0 1 0 0 1 1
C13	-5.2490234E-3	1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 0
C14	-8.1176758E-3	1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 0
C15	-8.4228516E-3	1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 0 0
C16	-5.2185059E-3	1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1
C17	1.2207031E-3	0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0
C18	9.1552734E-3	0 0 0 0 0 0 0 1 0 0 1 0 1 1 0 0 0
C19	1.5686035E-2	0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0
C20	1.7730713E-2	0 0 0 0 0 0 1 0 0 1 0 0 0 1 0 1 0
C21	1.3000488E-2	0 0 0 0 0 0 0 1 1 0 1 0 1 0 1 0 0
C22	1.4038086E-3	0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 0
C23	-1.4495850E-2	1 1 1 1 1 1 1 0 0 0 1 0 0 1 0 1 0
C24	-2.9541016E-2	1 1 1 1 1 1 1 0 0 0 0 1 1 1 0 0 0
C25	-3.7292480E-2	1 1 1 1 1 1 0 1 1 0 0 1 1 1 0 1 0
C26	-3.1829834E-2	1 1 1 1 1 1 0 1 1 1 1 1 0 1 1 0 1
C27	-9.8571777E-3	1 1 1 1 1 1 1 0 1 0 1 1 1 1 1 0 1
C28	2.7832031E-2	0 0 0 0 0 0 1 1 1 0 0 1 0 0 0 0 0
C29	7.5927734E-2	0 0 0 0 1 0 0 1 1 0 1 1 1 0 0 0 0
C30	1.2557983E-1	0 0 0 1 0 0 0 0 0 0 0 1 0 0 1 1 1
C31	1.6641235E-1	0 0 0 1 0 1 0 1 0 1 0 0 1 1 0 1 0
C32	1.8945313E-1	0 0 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0



FREQUENCY (NORMALIZED TO FOLDING FREQUENCY)

FIGURE C-8
FIR DIGITAL FILTER RESPONSE

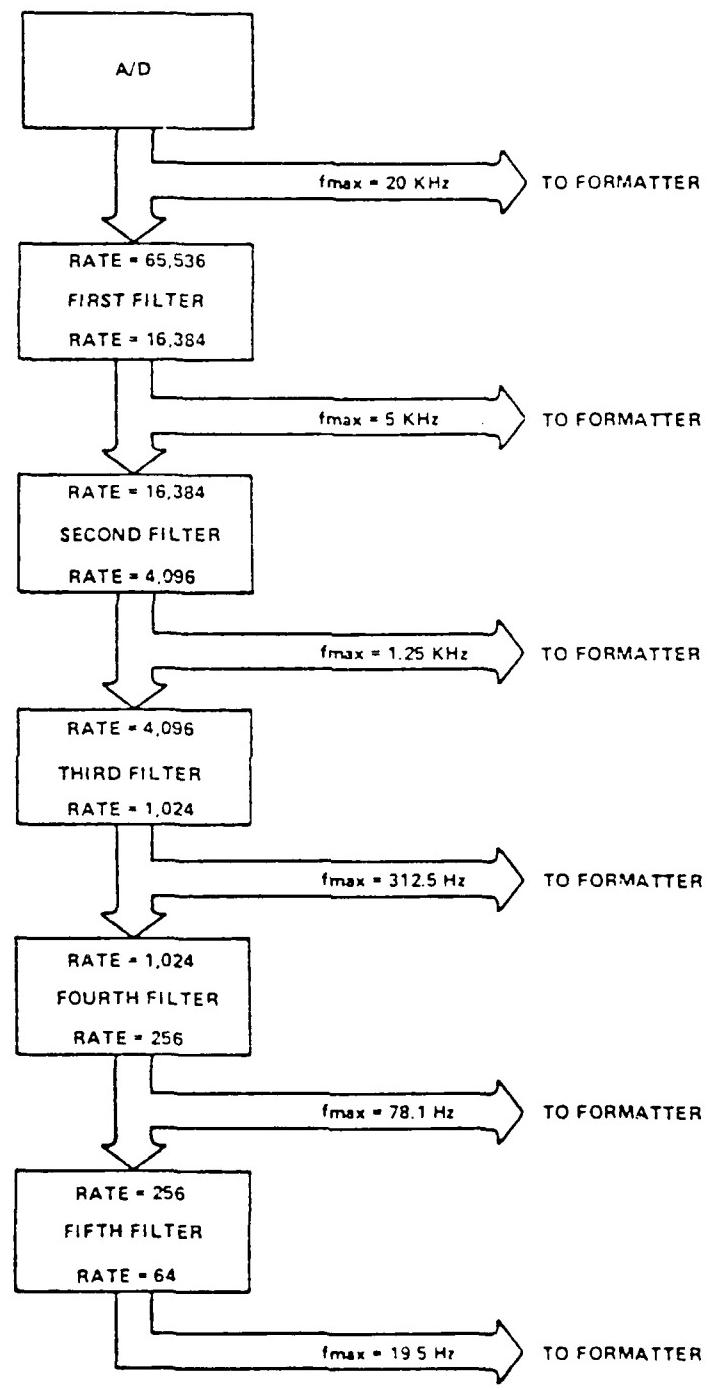


FIGURE C-9

CONCEPTUAL BLOCK DIAGRAM OF ALL DIGITAL FILTER SYSTEM

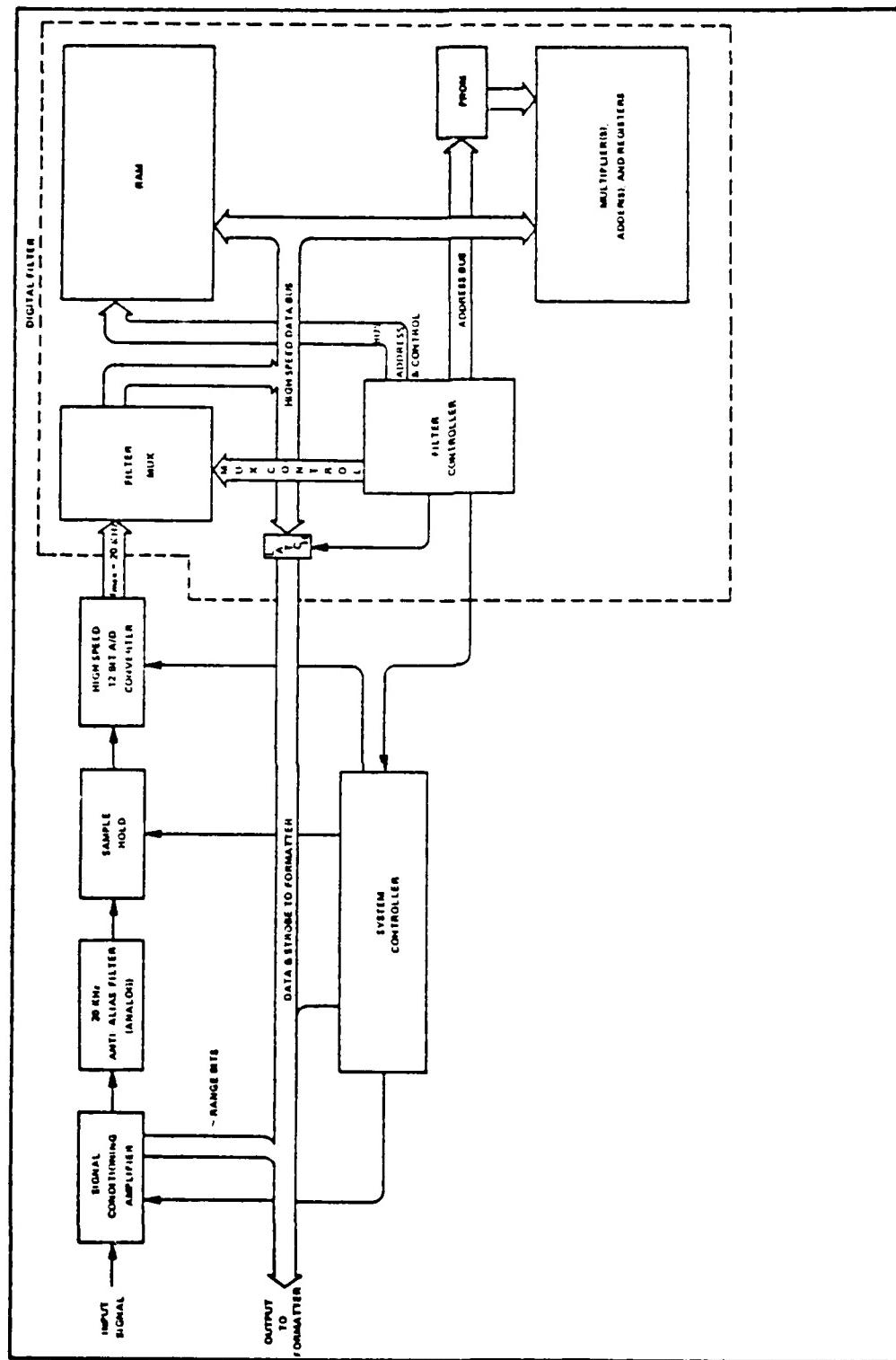


FIGURE C-10
FILTER SYSTEM BLOCK DIAGRAM

TABLE C-8
ARITHMETIC CHARACTERISTICS OF THE DIGITAL FILTERS
(one channel)

		Multiplication Rate (multiplications/second)	Memory Required (12 bit words)	Memory Access Rate (accesses/second)
1)	Fifth Filter	1,856	58	3,968
2)	Fourth Filter	7,424	58	15,872
3)	Third Filter	29,696	58	63,488
4)	Second Filter	118,784	58	253,952
5)	First Filter	475,136	58	1,015,808
6)	Total of lines 1 through 5	632,896	290	1,353,088
7)	Total of lines 1 through 4	157,760	232	337,280
8)	Total of lines 1 through 3	38,976	174	83,328
9)	Total of lines 1 and 2	9,280	116	19,840

Note: The above calculations are based on filters with 58 weights, 16 bit coefficients, and an A/D rate of 65,536 samples per second.

TABLE C-9
IMPLEMENTATION OF DIGITAL FILTERS AT $\times 10^3$ MULTIPLICATION RATE

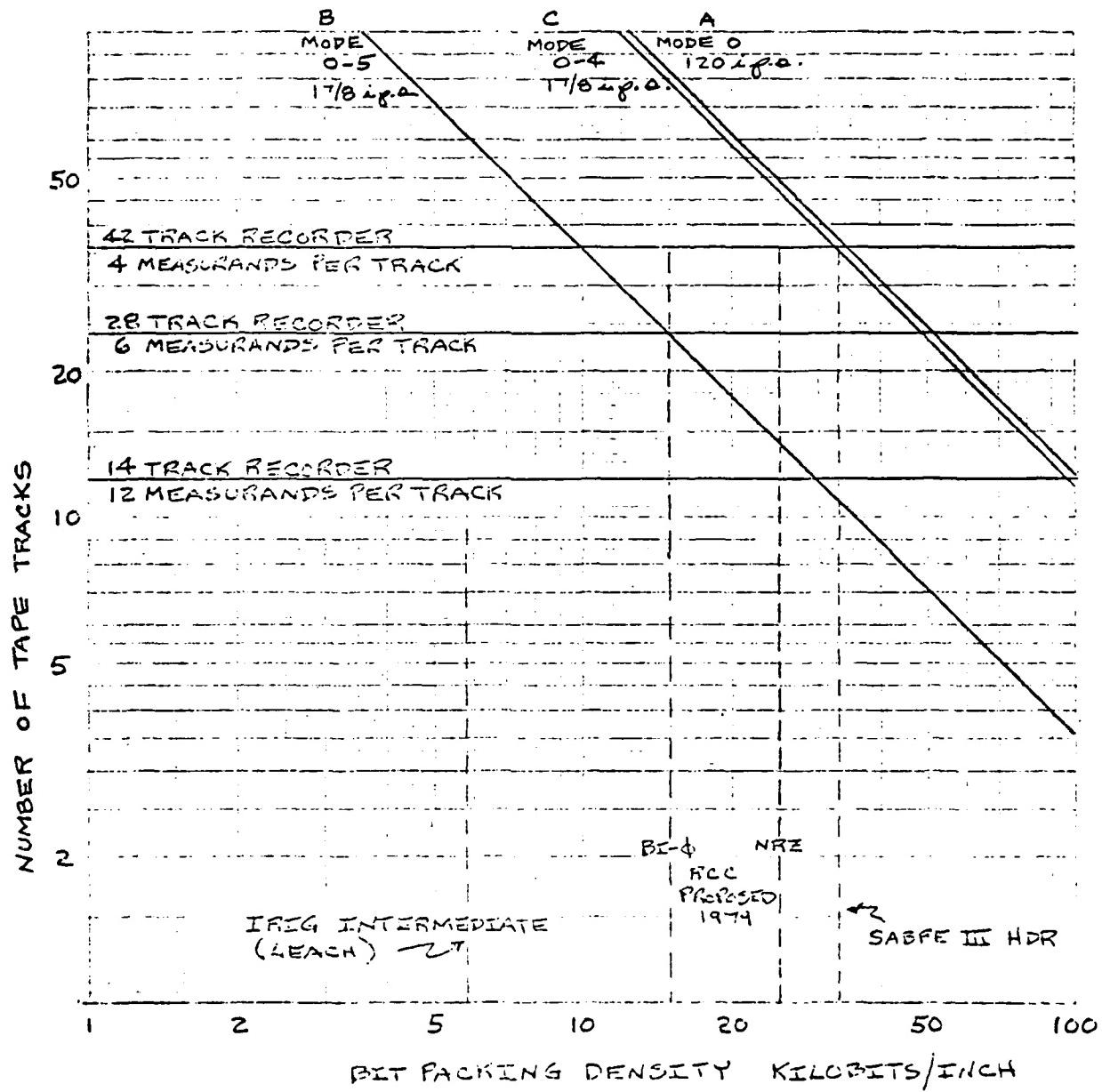
System	Type	Multiplications rate per channel	Memory Access rate (Hz) per channel	Chipspace per multiplier	Registers per system	RAM words required per system	RAM words per multiplier	Memory Access rate per channel per multiplier	Effective memory cycle time	Possible memory organization per register	Memory per system
A	6 Digital Filter	63.296	1,153,048	9.48 → 6	16	41,760	2,610	12,127,192	0.2 ns	16 Very Fast 16 × 4 RAMS	16 Very Fast 16 × 4 RAMS
B	4 Digital Filter	157,744	317,200	20.03 → 36	4	31,408	8,352	12,142,040	0.2 ns	(16 × 4 Fast) RAMS	(16 × 4 Fast) RAMS
C	4 Digital Filter	187,744	317,200	16	0	23,436	4,176	6,071,040	0.4 ns	(16 × 4 Fast) RAMS	(16 × 4 Fast) RAMS
D	3 Digital Filter	26,376	63,128	16.384 → 164	-	25,056	25,056	11,998,332	0.3 ns	76 Very Fast 16 × 4 RAMS	76 Very Fast 16 × 4 RAMS
E	2 Digital Filter	34,916	63,228	72	2	25,076	12,528	5,999,916	0.4 ns	76 Fast 16 × 4 RAMS	76 Fast 16 × 4 RAMS
F	3 Digital Filters	34,074	63,228	48	3	25,054	8,352	3,999,344	0.4 ns	(16K × 1 Dynamic) RAMS	(16K × 1 Dynamic) RAMS
G	2 Digital Filters	9,200	18,440	144	1	16,704	16,704	2,056,560	0.5 ns	16K × 1 Dynamic RAMS	16K × 1 Dynamic RAMS
H	2 Digital Filters	9,200	18,440	72	2	16,704	8,352	1,428,480	0.6 ns	16K × 1 Dynamic RAMS	16K × 1 Dynamic RAMS
I	1 Digital Filter	1,634	3,664	144	-	8,352	8,352	671,392	1.2 ns	16K × 1 Dynamic RAMS	12,16K × 1 Slow Dynamic RAMS

TABLE C-10
POWER CONSIDERATIONS FOR DIGITAL FILTERS

System	Typical RAM Power (Active/Standby)	Total RAM Power Per System	Total Multiply/Add Power Per System	Control System Logic	Control System & MUX Power (Est)	Minimum Total Power Estimate
A	850 mw/175 mw	57.6 W	96.0 W	ECL	45-65 W	199 W
B	850 mw/175 mw	27.0 W	24.0 W	ECL	40-60 W	91 W
C	400 mw/125 mw	21.6 W	48.0 W	S	25-35 W	95 W
D	850 mw/175 mw	15.15 W	6.0 W	ECL	40-55 W	61 W
E	400 mw/125 mw	11.4 W	12.0 W	S	25-35 W	48 W
F	180 mw/20 mw	6.48 W	18.0 W	S & LS	15-20 W	39 W
G	250 mw/25 mw	3.0 W	6.0 W	LS	8-12 W	17 W
H	130 mw/20 mw	3.12 W	12.0 W	LS	6-10 W	21 W
I	130 mw/20 mw	1.56 W	6.0 W	LS	4-8 W	12 W

TABLE C-11
BOARD AREA CONSIDERATIONS FOR DIGITAL FILTERS

System	Memory Area Estimate	Multiplexer-Adder Area Estimate	Control System & MUX Area	Minimum Total Area Estimate
A	$0.4 \times 144 = 57.6$	$12.0 \times 16 = 192.0$	85 - 120	$\sim 335 \text{ inches}^2$
B	$0.4 \times 108 = 43.2$	$12.0 \times 4 = 48.0$	80 - 110	$\sim 171 \text{ inches}^2$
C	$0.4 \times 120 = 48.0$	$12.0 \times 8 = 96.0$	70 - 90	$\sim 214 \text{ inches}^2$
D	$0.4 \times 75 = 30.0$	$12.0 \times 1 = 12.0$	80 - 100	$\sim 122 \text{ inches}^2$
E	$0.4 \times 75 = 31.2$	$12.0 \times 2 = 24.0$	70 - 90	$\sim 125 \text{ inches}^2$
F	$0.36 \times 36 \cong 13.0$	$12.0 \times 3 = 36.0$	65 - 80	$\sim 114 \text{ inches}^2$
G	$0.36 \times 12 \cong 4.3$	$12.0 \times 1 = 12.0$	52 - 68	$\sim 68 \text{ inches}^2$
H	$0.36 \times 24 \cong 8.7$	$12.0 \times 2 = 24.0$	44 - 60	$\sim 77 \text{ inches}^2$
I	$0.36 \times 12 \cong 4.3$	$12.0 \times 1 = 12.0$	36 - 52	$\sim 52 \text{ inches}^2$



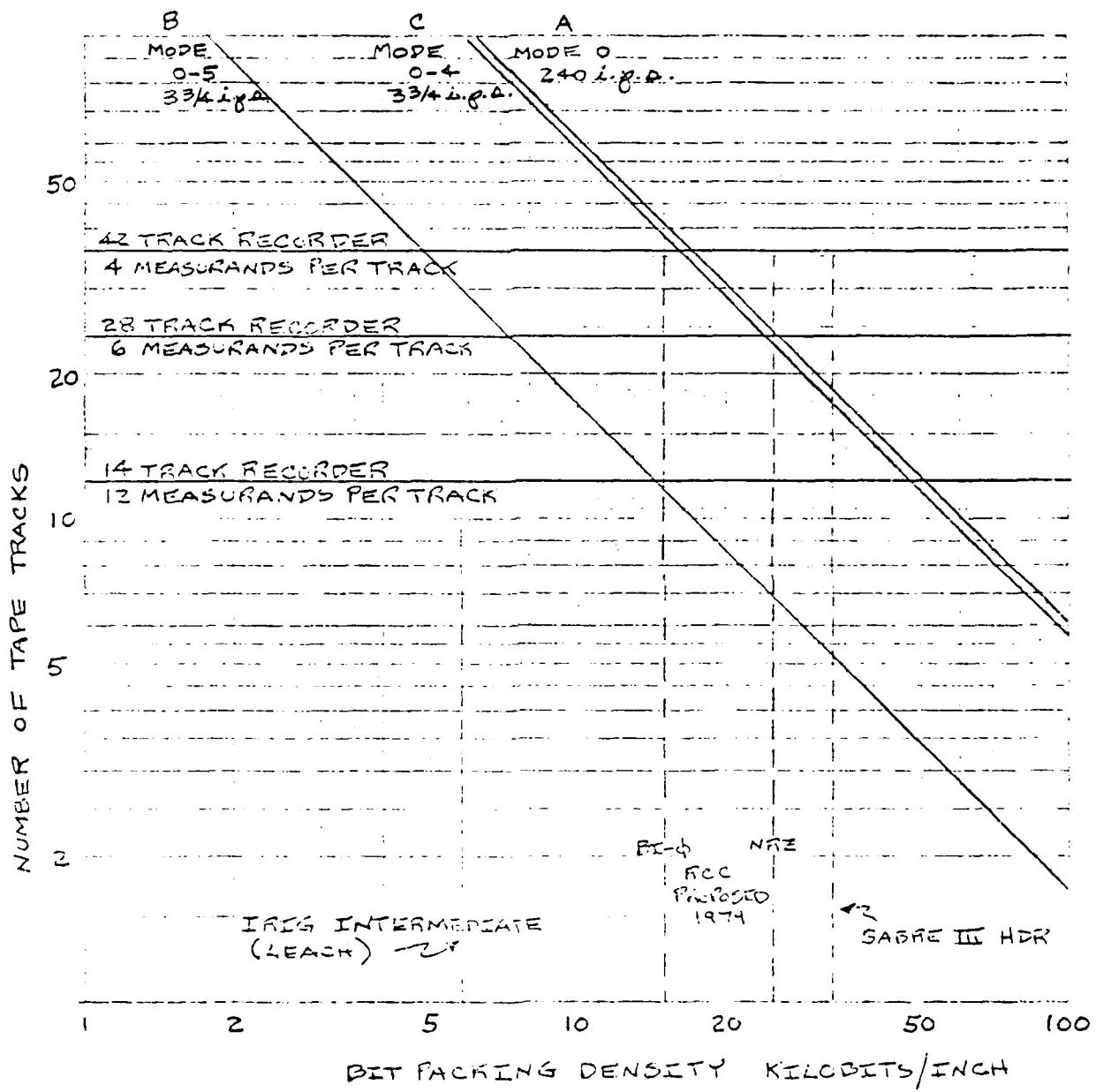


FIGURE C-12

TAPE RECORDER REQUIREMENTS 14 INCH REEL SIZE
3 3/4 IPS - 240 IPS 144 MEASURANDS

TABLE C-12
AIRCRAFT TAPE RECORDER CHARACTERISTICS

	<u>LEACH</u> <u>MTR-3200A2</u>	<u>BELL & HOWELL</u> <u>HARS 2000</u>	<u>BELL & HOWELL</u> <u>H-14</u>	<u>AMPEX</u> <u>AR-700</u>	<u>AMPEX</u> <u>AR-1700</u>	<u>SANGAMO</u> <u>SABRE XII</u>
REEL SIZE	8"	10 1/2"	14"	12 1/2"	14"	10 1/2"
SPEED RANGE	1 7/8 - 60 I.P.S.	1 7/8 - 60 I.P.S.	1 7/8 - 120 I.P.S.	1 7/8 - 60 I.P.S.	3 3/4 - 120 I.P.S.	15/16 - 120 I.P.S.
NO. OF TRACKS	14	14	14	14	14	28
BANDWIDTH	250 KHz @ 60 I.P.S.	1 MHz @ 60 I.P.S.	2 MHz @ 120 I.P.S.	1 MHz @ 60 I.P.S.	2 MHz @ 120 I.P.S.	2 MHz @ 120 I.P.S.
VOL'UE	1.27 ft ³	0.56 ft ³	1.97 ft ³	1.23 ft ³	2.27 ft ³	1.73 ft ³
WEIGHT	< 100 lb	38 lb	74 lb	48 lb	76 lb	69 lb
POWER	< 100W.	115W.	280W.	175W. (+250W.*)	300W. (+250W.*)	270W.

* HEATER POWER

TABLE C-13
GROUND (PORTABLE AND LABORATORY) TAPE RECORDER CHARACTERISTICS

	SANGAMO <u>SABRE III</u>	HONEYWELL <u>101</u>	SANGAMO <u>SABRE X</u>	HONEYWELL <u>96C</u>
TYPE	PORTABLE	PORTABLE	LABORATORY	LABORATORY
REEL SIZE	14" - 16"	10 1/2" - 15"	10 1/2" - 16"	10 1/2" - 16"
SPEED RANGE	15/16 - 120 1.p.s.	15/16 - 120 1.p.s.	15/32 - 240 1.p.s.	15/16 - 240 1.p.s.
NO. OF TRACKS	14	14	7 - 48	14*
BANDWIDTH	2 MHz @ 120 1.p.s.	2 MHz @ 120 1.p.s.	4 MHz @ 240 1.p.s.	4 MHz @ 240 1.p.s.
VOLUME	3.19 ft ³	3.95 ft ³	-	-
WEIGHT	100 lb	100 lb	-	-
POWER	-	480W.	-	-

* CAN BE UPGRADED TO 42 TRACKS BY SPIN PHYSICS, INC.

TABLE C-14
COMPARISONS OF AUTO VS. PROGRAMMED GAIN SYSTEMS

	<u>AGR</u>	<u>PG</u>
• size	12 sq. in.	8 sq. in.*
• power	530 mw	340 mw*
• gain range	70 db dynamic	70 db programmed
• versatility	excellent	very good
• calibration	difficult	relatively simple
• ease of use	excellent	very good
• bit overhead	approx. 20%	none
• multiplex capability	difficult	normal

*does not include storage requirements for gain select bits

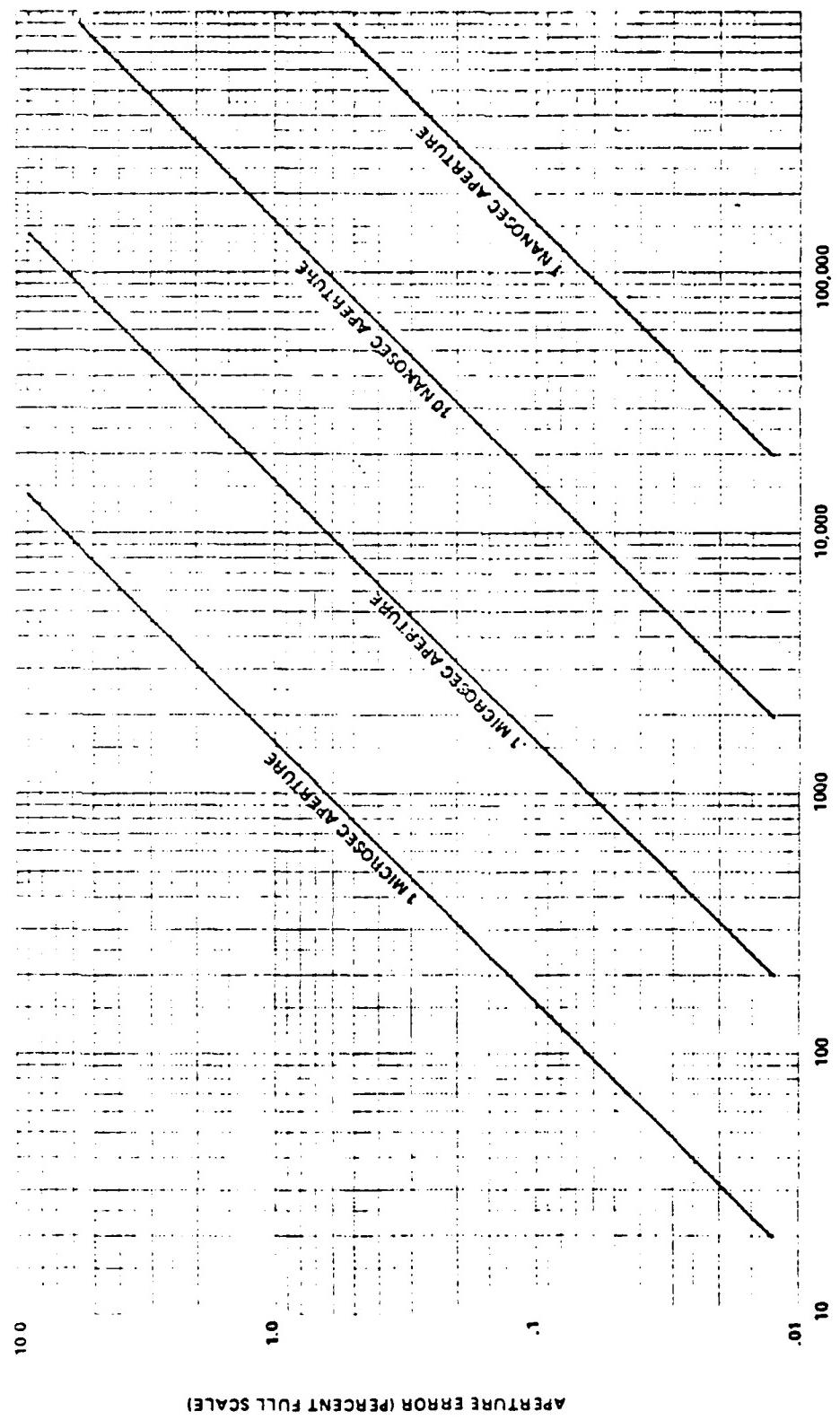


FIGURE C-13

APERTURE ERROR VERSUS SIGNAL FREQUENCY

TABLE C-15
COMPARISONS OF VARIOUS SAMPLE/HOLD CIRCUITS

	<u>Monolithic</u>	<u>Discrete</u>	<u>Hybrid</u>
• size	0.2 sq. in.	2 sq. in.	1.2 sq. in.
• power	150 mw	580 mw	1.6 watts
• cost	\$60	\$200	\$320
• aperture time	50 ns	20 ns	20 ps

TABLE C-16
COMPARISONS OF A/D CONVERSION TECHNIQUES

	<u>Successive Approx.</u>	<u>Parallel (Subranging)</u>
• size	6 sq. in. (discrete) 1.6 sq. in. (hybrid)	8 sq. in.
• power	1.5 to 2 watts	7 watts
• encode time	1.2 us to 1.8 us	200 ns
• multiplexed capacity	8 to 12 channels	60 to 80 channels
• calibration	simple	very difficult
• complexity	moderate	high

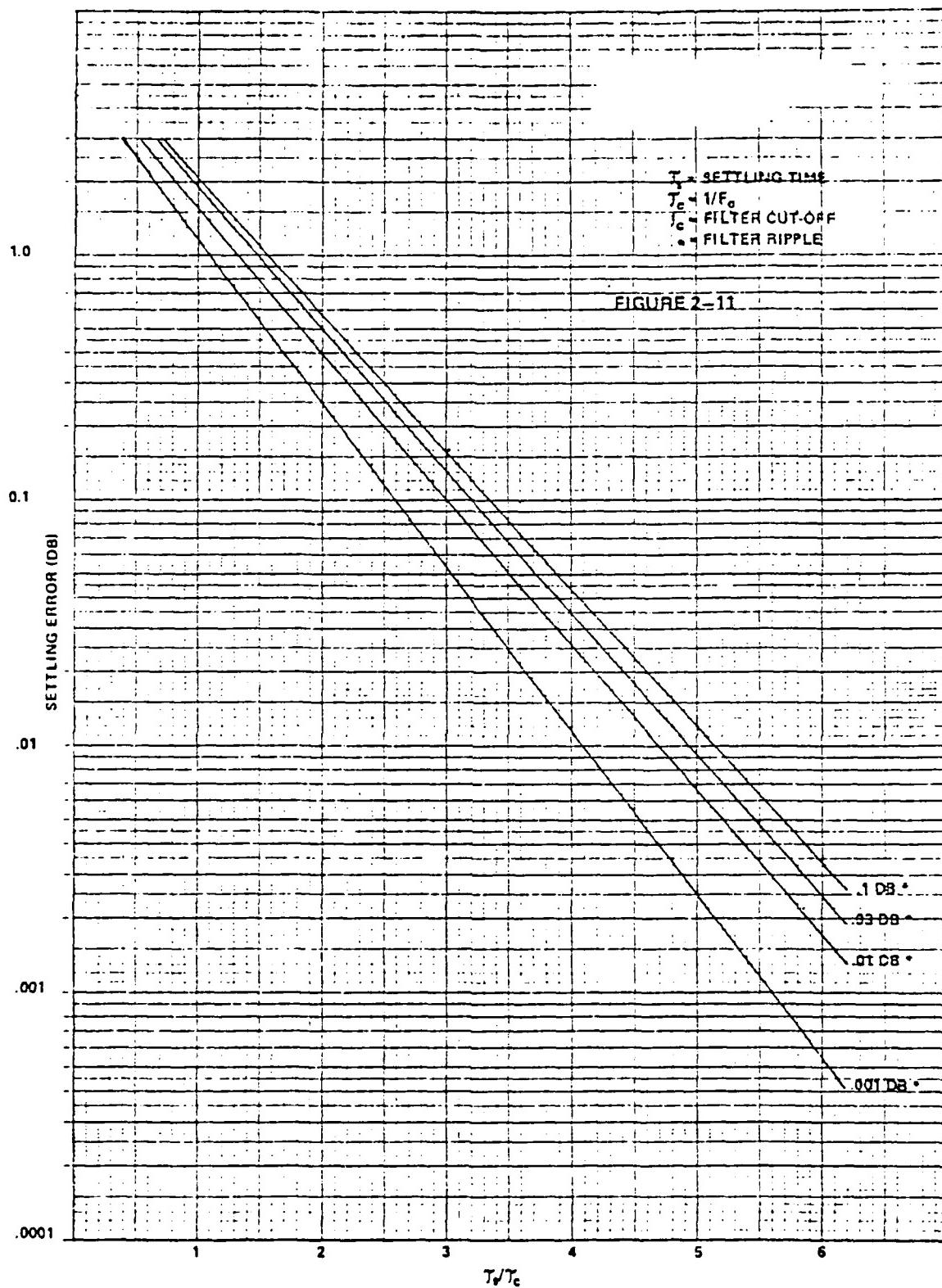


FIGURE 2-11

FIGURE C-14
SETTLING ERROR OF 8-POLE LOWPASS CHEBYSHEV FILTER TO UNIT STEP INPUT

TABLE C-17
AFTOL/FBG PCM System - Editing Considerations

Operating Mode Definition		Analysis Transform Size	Total Record Time	Required data record length for analysis			Disk capacity (1/2 256 MB) number of analysis time series			Disk capacity (1/2 256 MB) % of total recorded data	
Filters	Samples per filter sampled			1 Average	16 Averages	64 Averages	1 Average	16 Averages	64 Averages	1 Average	16 Averages
B 0-5	64 512 2048	64 512 2048	8 hrs.	1.333 10.661 42.656	21.328 170.625 632.5	85.313 682.5 2730	166.666 20.833 5208	10,416 1302 325	2604 325 81	5.41	
C 0-4	64 512 2048	64 512 2048	8 hrs.	0.333 2.664 10.656	5.328 42.625 170.5	21.313 170.5 682	260,000 25,000 6250	12,500 1562 390	3125 390 97	1.62	
A 0	-	512 2048	7.5 min.	0.00728 0.03125 0.25	0.125 0.5 4.0	0.5 2.0 16	125,000 31,250 3906	7812 1953 244	1953 488 61	1.53	
E 1-5	64 512 2048	64 512 2048	8 hrs.	1.332 10.656 42.625	21.313 170.5 682	85.25 682 2728	200,000 25,000 6250	12,500 1562 390	3125 390 97	6.41	
F 1-4	64 512 2048	64 512 2048	8 hrs.	0.332 2.656 10.625	5.313 42.5 170	21.25 170 610	250,000 31250 7812	16,625 1953 488	3906 488 122	2.05	
D 1	-	512 2048	7.5 min.	0.03125 0.125 1.0	0.5 2.0 16	2.0 8.0 64	125,000 31,250 3906	7812 1953 244	1953 488 61	6.04	
H 2-5	64 512 2048	64 512 2048	8 hrs.	1.328 10.625 42.5	21.25 170 680	85 680 2720	250,000 31250 7812	16,625 1953 488	3906 488 122	8.05	
I 2-4	64 512 2048	64 512 2048	8 hrs.	0.328 2.625 10.5	5.25 42 168	21 168 612	333,333 41,666 10,416	20,833 2604 651	52038 651 162	2.64	
C 2	-	512 2048	7.5 min.	0.125 0.5 4.0	2.0 8.0 64	8.0 32 256	125,000 31,250 3906	7812 1953 244	1953 488 61	24.12	

TABLE C-18
DATA PLAYBACK, DECOMMUTATION, AND EDITING
(USING 42 TRACK RECORDER)

MODE A: 20 KHZ RESPONSE, 7.5 MINUTES RECORD TIME, 240 I.P.S. RECORD SPEED, 264 WORD PCM FRAME, 36 DATA TRACKS, 4 MEASURANDS PER TRACK,
 18.0 KILOBITS PER INCH

REPRODUCE SPEED	PER PASS PLAYBACK TIME	PER TRACK DECIM. RATE	ANALOG RESPONSE (0/A)	TOTAL PLAYBACK TIME (INCLUDES R/WIND)		
				1 DECIM.	2 DECIM.	3 DECIM.
240 I.P.S.	.125 hr	4.31 Mb/sec	20 kHz	8.88 hrs	4.38 hrs	2.88 hrs
120 I.P.S.	.25 hr	2.16 Mb/sec	10 kHz	13.38 hrs	6.63 hrs	4.38 hrs
60 I.P.S.	.5 hr	1.09 Mb/sec	5 kHz	22.38 hrs	11.13 hrs	7.38 hrs
30 I.P.S.	1 hr	0.541 Mb/sec	2.5 kHz	40.38 hrs	20.13 hrs	13.38 hrs
15 I.P.S.	2 hr	0.270 Mb/sec	1.25 kHz	76.38 hrs	38.13 hrs	25.38 hrs

MODE C: 20 KHZ RESPONSE, 8 HOURS RECORD TIME, 3.75 I.P.S. RECORD SPEED, 264 WORD PCM FRAME, 36 DATA TRACKS, 4 MEASURANDS PER TRACK,
 16.9 KILOBITS PER INCH

REPRODUCE SPEED	PER PASS PLAYBACK TIME	PER TRACK DECIM. RATE	ANALOG RESPONSE (0/A)	TOTAL PLAYBACK TIME (INCLUDES R/WIND)		
				1 DECIM.	2 DECIM.	3 DECIM.
240 I.P.S.	.125 hr	4.06 Mb/sec	18.8 kHz	8.88 hrs	4.38 hrs	2.88 hrs
120 I.P.S.	.25 hr	2.03 Mb/sec	9.38 kHz	13.38 hrs	6.63 hrs	4.38 hrs
60 I.P.S.	.5 hr	1.01 Mb/sec	4.69 kHz	22.38 hrs	11.13 hrs	7.38 hrs
30 I.P.S.	1 hr	0.507 Mb/sec	2.35 kHz	40.38 hrs	20.13 hrs	13.38 hrs
15 I.P.S.	2 hr	0.254 Mb/sec	1.17 kHz	76.38 hrs	38.13 hrs	25.38 hrs

MODE B: 20 KHZ RESPONSE, 8 HOURS RECORD TIME, 3.75 I.P.S. RECORD SPEED, 264 WORD PCM FRAME, 9 DATA TRACKS, 16 MEASURANDS PER TRACK,
 20.3 KILOBITS PER INCH

REPRODUCE SPEED	PER PASS PLAYBACK TIME	PER TRACK DECIM. RATE	ANALOG RESPONSE (0/A)	TOTAL PLAYBACK TIME (INCLUDES R/WIND)		
				1 DECIM.	2 DECIM.	3 DECIM.
240 I.P.S.	.125 hr	4.87 Mb/sec	5.63 kHz	2.13 hrs	1.00 hrs	0.63 hrs
120 I.P.S.	.25 hr	2.43 Mb/sec	2.81 kHz	3.25 hrs	1.56 hrs	1.00 hrs
60 I.P.S.	.5 hr	1.22 Mb/sec	1.41 kHz	5.5 hrs	2.69 hrs	1.75 hrs
30 I.P.S.	1 hr	0.603 Mb/sec	0.703 kHz	10.0 hrs	4.96 hrs	3.25 hrs
15 I.P.S.	2 hr	0.304 Mb/sec	0.352 kHz	19.0 hrs	9.44 hrs	6.25 hrs

TABLE C-19
DATA PLAYBACK, DECOMMUTATION, AND EDITING
(USING 28 TRACK RECORDER)

MODE A: 20 KHZ RESPONSE, 7.5 MINUTES RECORD TIME, 240 I.P.S. RECORD SPEED, 392 WORD PCM FRAME, 24 DATA TRACKS, 6 MEASURANDS PER TRACK,
 26.8 KILOBITS PER INCH

REPRODUCE SPEED	PER PASS PLAYBACK TIME	PER TRACK DECOR. RATE	ANALOG RESPONSE (D/A)	TOTAL PLAYBACK TIME (INCLUDES REMIND)		
				1 DECIM.	2 DECIM.	3 DECIM.
240 I.P.S.	.125 hr	6.42 Mb/sec	20 KHz	5.88 hrs	2.88 hrs	1.88 hrs
120 I.P.S.	.25 hr	3.21 Mb/sec	10 KHz	8.86 hrs	4.38 hrs	2.88 hrs
60 I.P.S.	.5 hr	1.61 Mb/sec	5 KHz	14.88 hrs	7.38 hrs	4.88 hrs
30 I.P.S.	1 hr	0.803 Mb/sec	2.5 KHz	26.88 hrs	13.38 hrs	8.88 hrs
15 I.P.S.	2 hr	0.401 Mb/sec	1.25 KHz	50.88 hrs	25.38 hrs	16.88 hrs
7.5 I.P.S.	4 hr	0.201 Mb/sec	0.625 KHz	98.88 hrs	49.38 hrs	32.88 hrs

MODE C: 20 KHZ RESPONSE, 8 HOURS RECORD TIME, 3.75 I.P.S. RECORD SPEED, 392 WORD PCM FRAME, 24 DATA TRACKS, 6 MEASURANDS PER TRACK,
 25.1 KILOBITS PER INCH

REPRODUCE SPEED	PER PASS PLAYBACK TIME	PER TRACK DECOR. RATE	ANALOG RESPONSE (D/A)	TOTAL PLAYBACK TIME (INCLUDES REMIND)		
				1 DECIM.	2 DECIM.	3 DECIM.
240 I.P.S.	.125 hr	6.03 Mb/sec	18.8 KHz	5.88 hrs	2.88 hrs	1.88 hrs
120 I.P.S.	.25 hr	3.01 Mb/sec	9.38 KHz	8.88 hrs	4.38 hrs	2.88 hrs
60 I.P.S.	.5 hr	1.51 Mb/sec	4.69 KHz	14.88 hrs	7.38 hrs	4.88 hrs
30 I.P.S.	1 hr	0.753 Mb/sec	2.35 KHz	26.88 hrs	13.38 hrs	8.88 hrs
15 I.P.S.	2 hr	0.377 Mb/sec	1.17 KHz	50.88 hrs	25.38 hrs	16.88 hrs

MODE B: 20 KHZ RESPONSE, 8 HOURS RECORD TIME, 3.75 I.P.S. RECORD SPEED, 392 WORD PCM FRAME, 12 DATA TRACKS, 12 MEASURANDS PER TRACK,
 15.1 KILOBITS PER INCH

REPRODUCE SPEED	PER PASS PLAYBACK TIME	PER TRACK DECOR. RATE	ANALOG RESPONSE (D/A)	TOTAL PLAYBACK TIME (INCLUDES REMIND)		
				1 DECIM.	2 DECIM.	3 DECIM.
240 I.P.S.	.125 hr	3.61 Mb/sec	5.63 KHz	2.88 hrs	1.38 hrs	0.88 hrs
120 I.P.S.	.25 hr	1.81 Mb/sec	2.61 KHz	4.38 hrs	2.13 hrs	1.18 hrs
60 I.P.S.	.5 hr	0.903 Mb/sec	1.41 KHz	7.38 hrs	3.63 hrs	2.18 hrs
30 I.P.S.	1 hr	0.452 Mb/sec	0.703 KHz	13.38 hrs	6.63 hrs	4.18 hrs
15 I.P.S.	2 hr	0.226 Mb/sec	0.352 KHz	25.38 hrs	12.63 hrs	8.18 hrs

TABLE C-20

TOTAL PROCESSING TIMES IN MILLISECONDS FOR DEC
PDP 11/34A AND FPS AP120B CALCULATIONS AND DATA TRANSFERS

TOTAL # 16 BIT TRANSFERS	N ₀	N ₁	#16 BIT TRANSFERS IN SAMPLE							
		64	128	256	512	1024	2048	4096	8192	16384
.98	64	B	14.6	N/A						
		L	14.7	N/A						
2.0	128	B	15.0	14.9	N/A					
		L	15.1	15.0	N/A					
3.9	256	B	15.9	15.8	15.7	N/A				
		L	16.1	15.9	15.8	N/A				
7.8	512	B	17.7	17.4	17.3	17.2	N/A			
		L	18.0	17.6	17.4	17.3	N/A			
15.6	1024	B	21.3	20.7	20.4	20.3	20.2	N/A		
		L	21.9	21.0	20.6	20.4	20.3	N/A		
31.3	2048	B	28.5	27.3	26.7	26.5	26.3	26.3	N/A	
		L	29.6	27.9	27.0	26.6	26.4	26.3	N/A	
62.5	4096	B	42.8	40.5	39.4	38.7	38.5	38.4	38.3	N/A
		L	45.1	41.6	39.9	39.0	38.6	38.4	38.3	N/A
125	8192	B	72.2	67.5	65.1	64.0	63.4	63.1	63.0	62.9
		L	76.7	69.8	66.3	64.6	63.7	63.3	63.1	63.0
250	16384	B	130.1	120.8	116.1	113.7	112.6	112.0	111.7	111.6
		L	139.0	125.3	118.4	114.9	113.2	112.3	111.9	111.7
500	32768	B	245.9	227.3	218.0	213.3	210.9	209.8	209.2	208.9
		L	263.7	236.2	222.5	215.6	212.1	210.4	209.5	209.1
AVAILABLE REAL TIME MODE A										

NOTE: B IS BRUTE FORCE IMPLEMENTATION
L IS LOOP IMPLEMENTATION
N/A IS NOT APPLICABLE

TABLE C-21

TOTAL PROCESSING TIMES IN MILLISECONDS FOR
 DEC VAX 11/780 RUNNING VMS WITHOUT OPTIMIZATION
 AND FPS AP120B CALCULATIONS AND DATA TRANSFERS

TOTAL # 16 BIT TRANSFERS	N_0	N_1	#16 BIT TRANSFERS IN SAMPLE								
			64	128	256	512	1024	2048	4096	8192	16384
.98	64	B	9.4	N/A							
		L	9.5	N/A							
2.0	128	B	10.3	10.2	N/A						
		L	10.4	10.3	N/A						
3.9	256	B	11.1	11.0	10.9	N/A					
		L	11.3	11.1	11.0	N/A					
7.8	512	B	13.1	12.8	12.7	12.6	N/A				
		L	13.4	13.0	12.8	12.7	N/A				
15.6	1024	B	17.8	16.5	16.3	16.2	16.1	N/A			
		L	18.4	16.9	16.5	16.3	16.2	N/A			
31.3	2048	B	25.7	24.6	23.4	23.2	23.0	23.0	N/A		
		L	26.8	25.2	23.7	23.3	23.1	23.0	N/A		
62.5	4096	B	41.9	39.4	38.4	37.1	36.9	36.8	36.7	N/A	
		L	44.2	40.5	38.9	37.4	37.0	36.8	36.7	N/A	
125	8192	B	74.6	69.5	66.9	65.9	64.7	64.4	64.3	64.2	N/A
		L	79.1	71.8	68.1	66.5	65.0	64.6	64.4	64.3	N/A
250	16384	B	139.7	129.4	124.3	121.7	120.7	119.5	119.2	119.1	119.0
		L	148.6	133.9	126.6	122.9	121.3	119.8	119.4	119.2	119.1
500	32768	B	269.3	248.8	238.5	233.4	230.8	229.8	228.6	228.3	228.2
		L	287.1	257.7	243.0	235.7	232.0	230.4	228.9	228.5	228.3

AVAILABLE
 REAL TIME
 MODE A

NOTE: B IS BRUTE FORCE IMPLEMENTATION
 L IS LOOP IMPLEMENTATION
 N/A IS NOT APPLICABLE

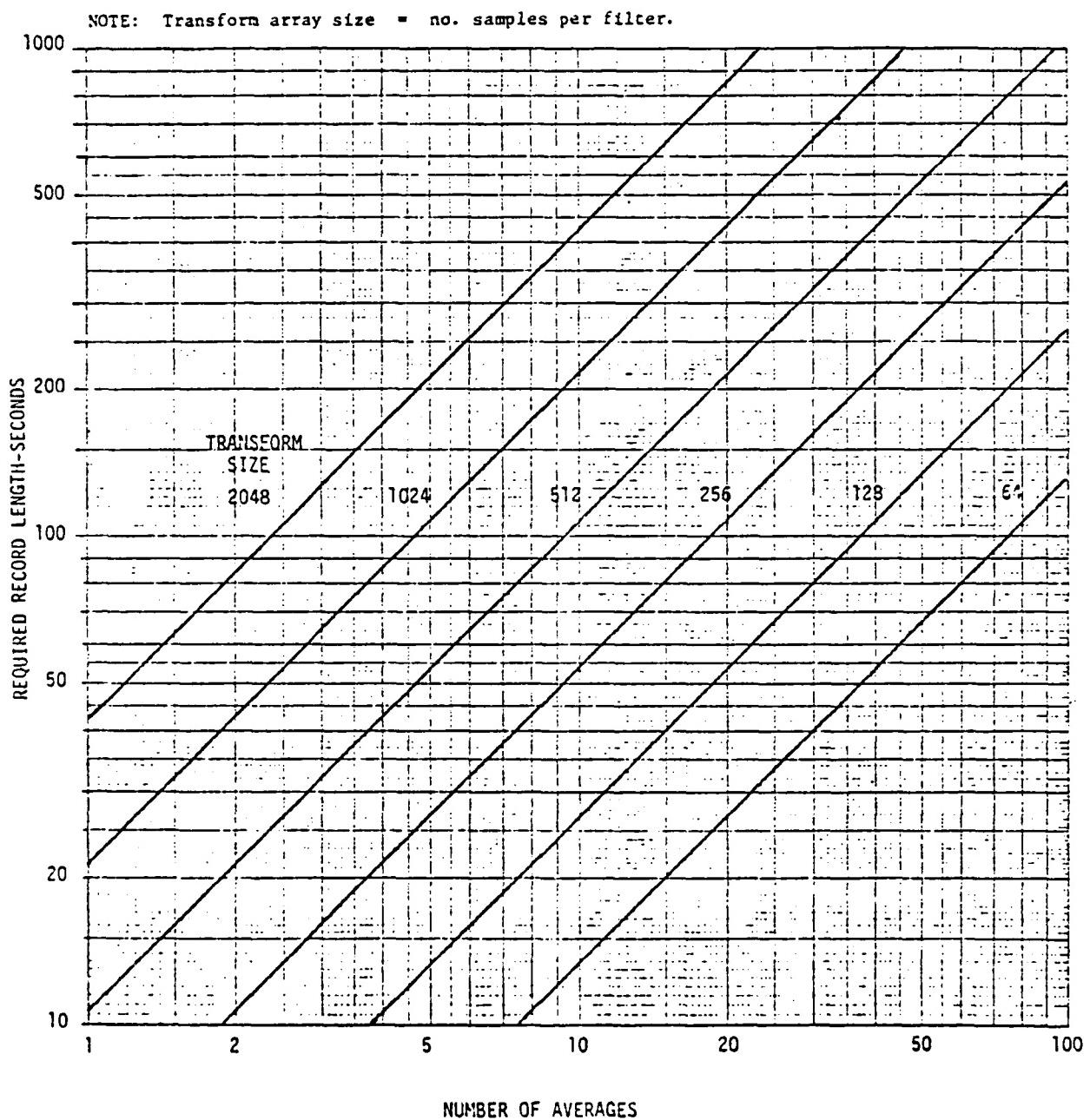


FIGURE C-15
MULTIPLE FILTER ENCODING
FILTERS SAMPLED 0-5 REQUIRED RECORD LENGTH AS A FUNCTION
OF NO. OF AVERAGES AND TRANSFORM ARRAY SIZE

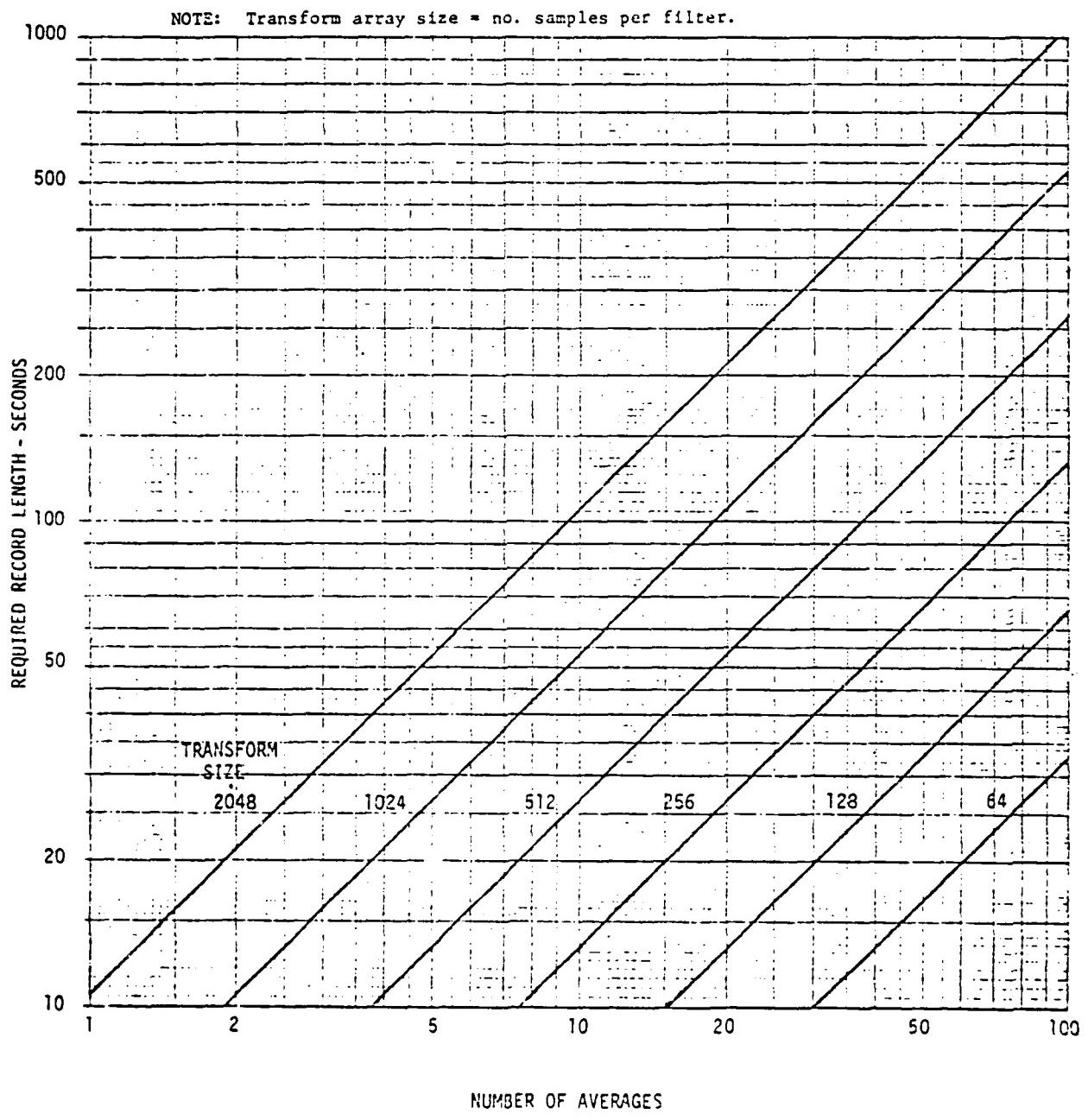


FIGURE C-16
MULTIPLE FILTER ENCODING
FILTERS SAMPLED 0-4 REQUIRED RECORD LENGTH AS A FUNCTION
OF NO. OF AVERAGES AND TRANSFORM ARRAY SIZE

TABLE C-22
MULTIPLE FILTER ENCODING

FREQUENCY RESOLUTION				SAMPLES/FILTER			
Δf_5	Δf_4	Δf_3	Δf_2	Δf_1	Δf_o	N	HERTZ
.03125	.125	.5	2	8	32	2048	20K
						1024	
				16	64		
						512	
						256	
						128	
						64	
						32	
						16	
						8	
						4	
						2	
						1	
							5K
							1250
							312.5
							78.1
							19.5

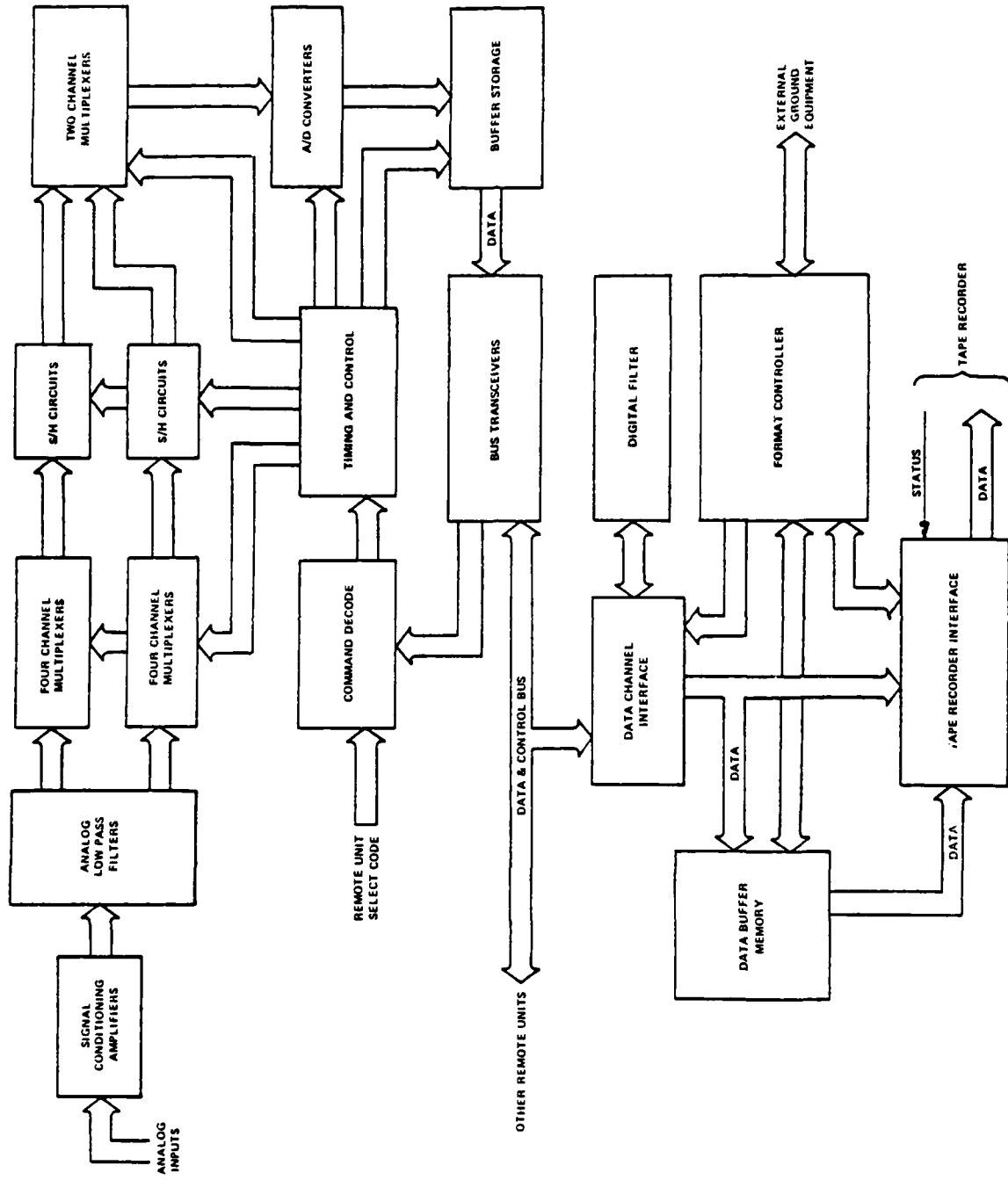


FIGURE G-17
BLOCK DIAGRAM OF DISTRIBUTED PCM SYSTEM

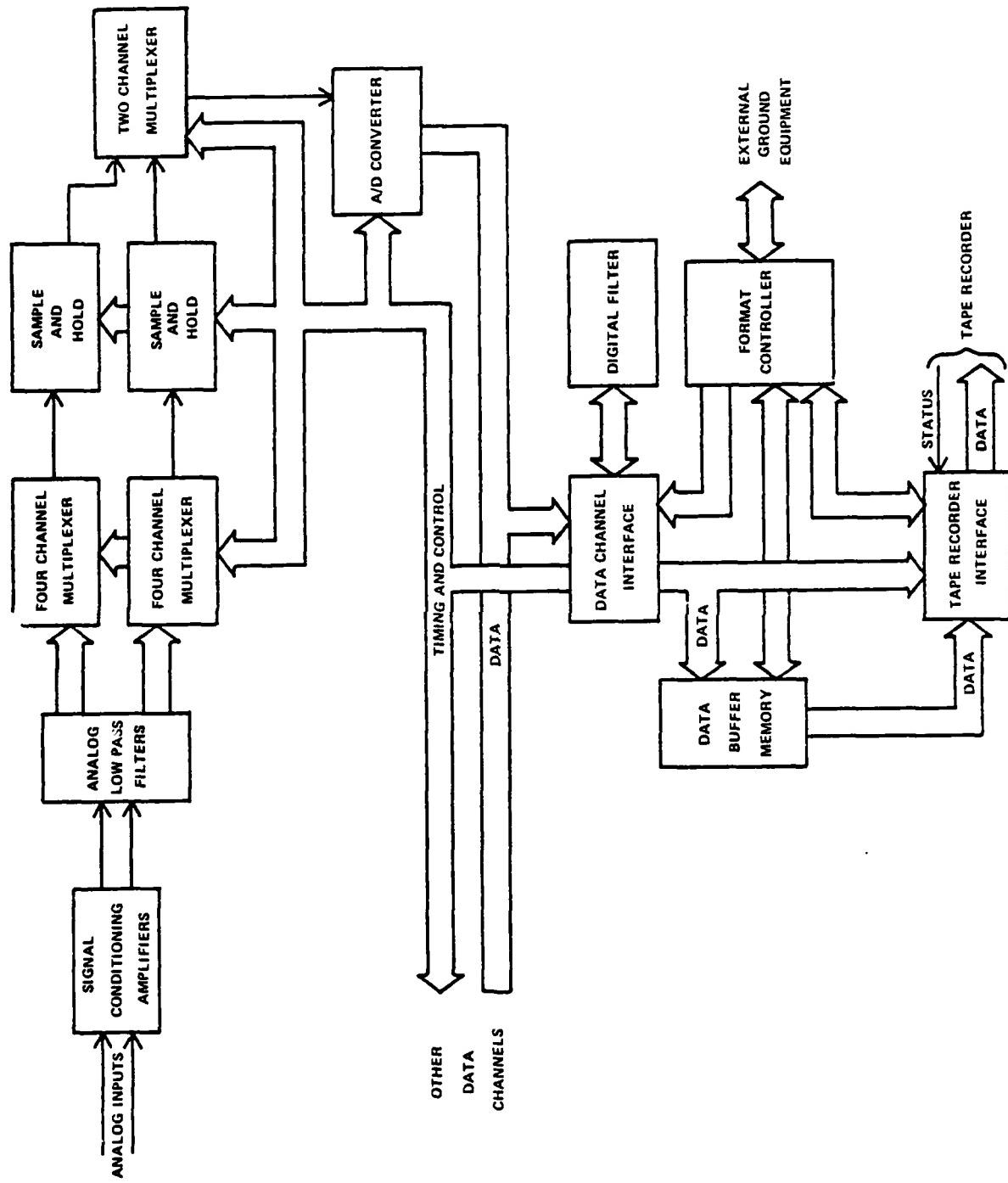


FIGURE C-18
BLOCK DIAGRAM OF CENTRALIZED PCM SYSTEM

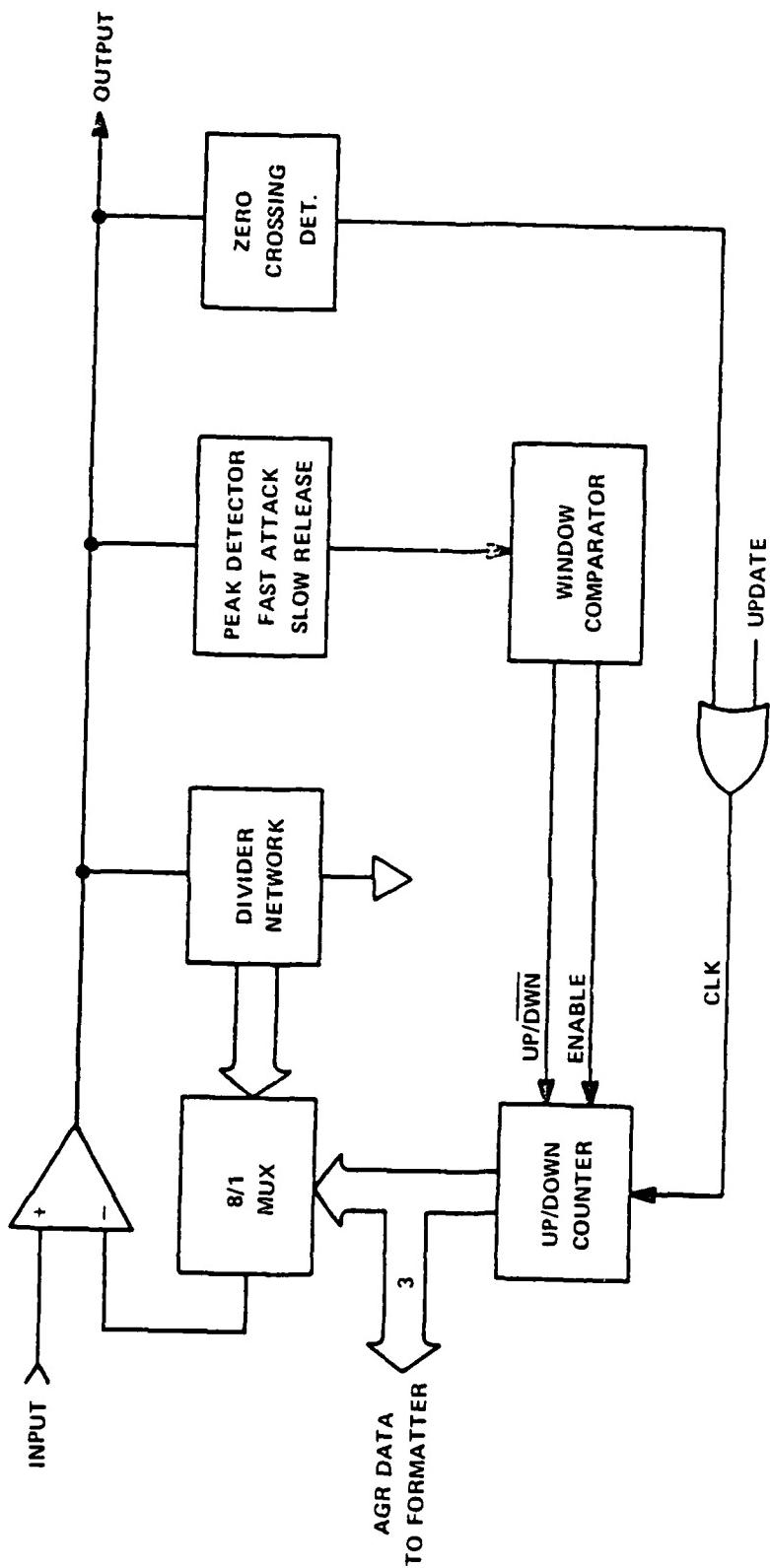


FIGURE C-19
AGR AUTO GAIN RANGING AMPLIFIER

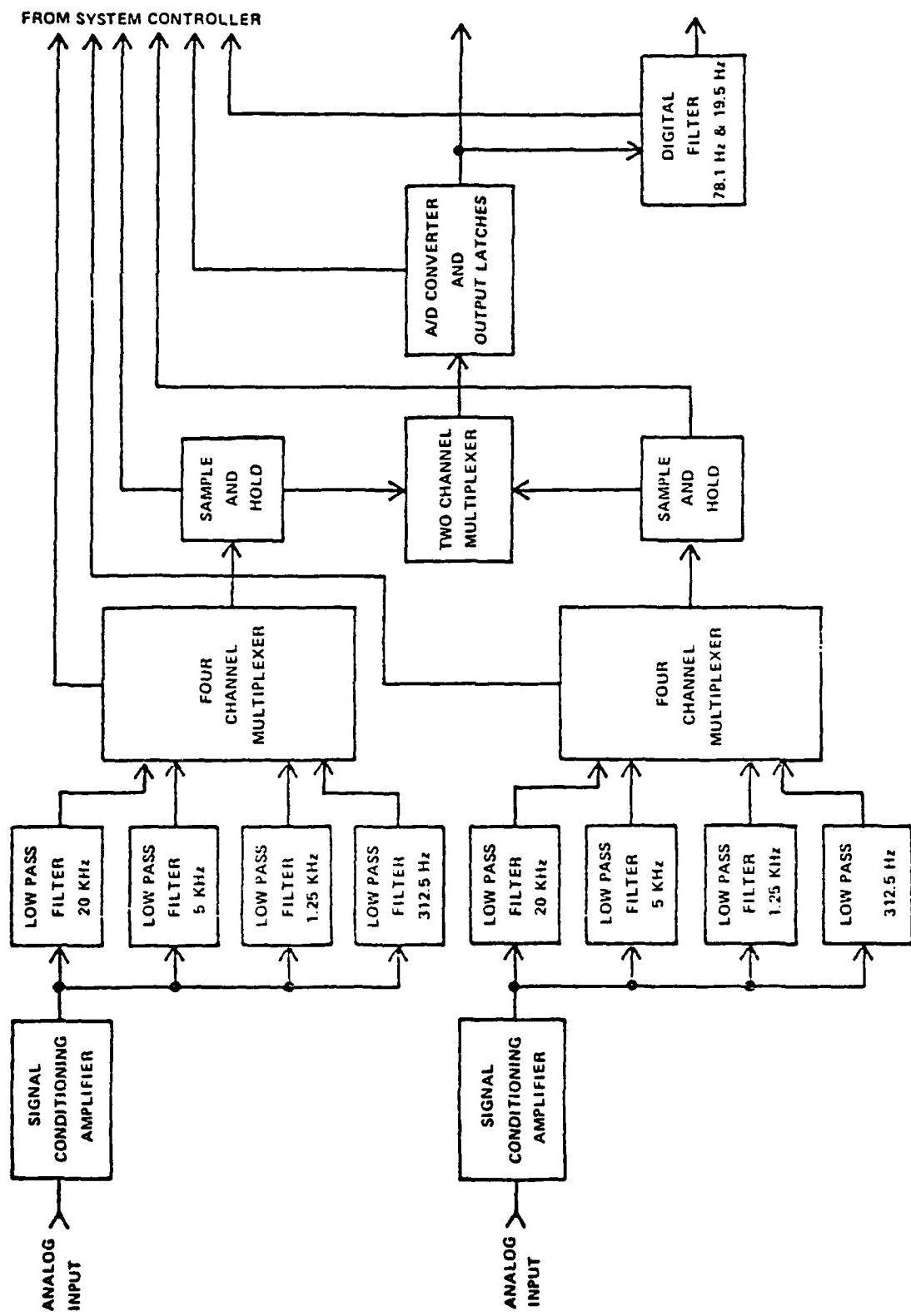


FIGURE C-20
ANALOG/DIGITAL FILTER SUBSYSTEM

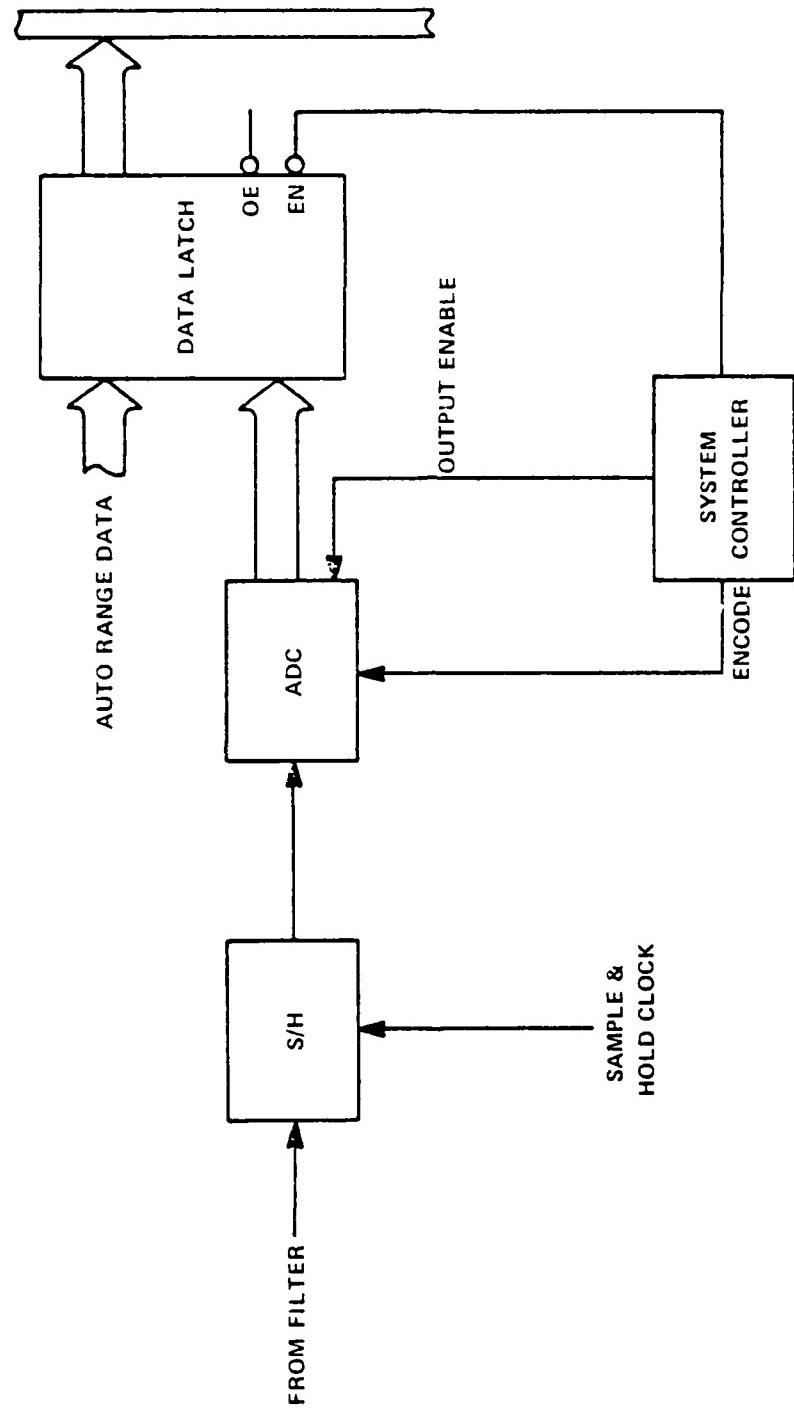


FIGURE C-21
DEDICATED ADC

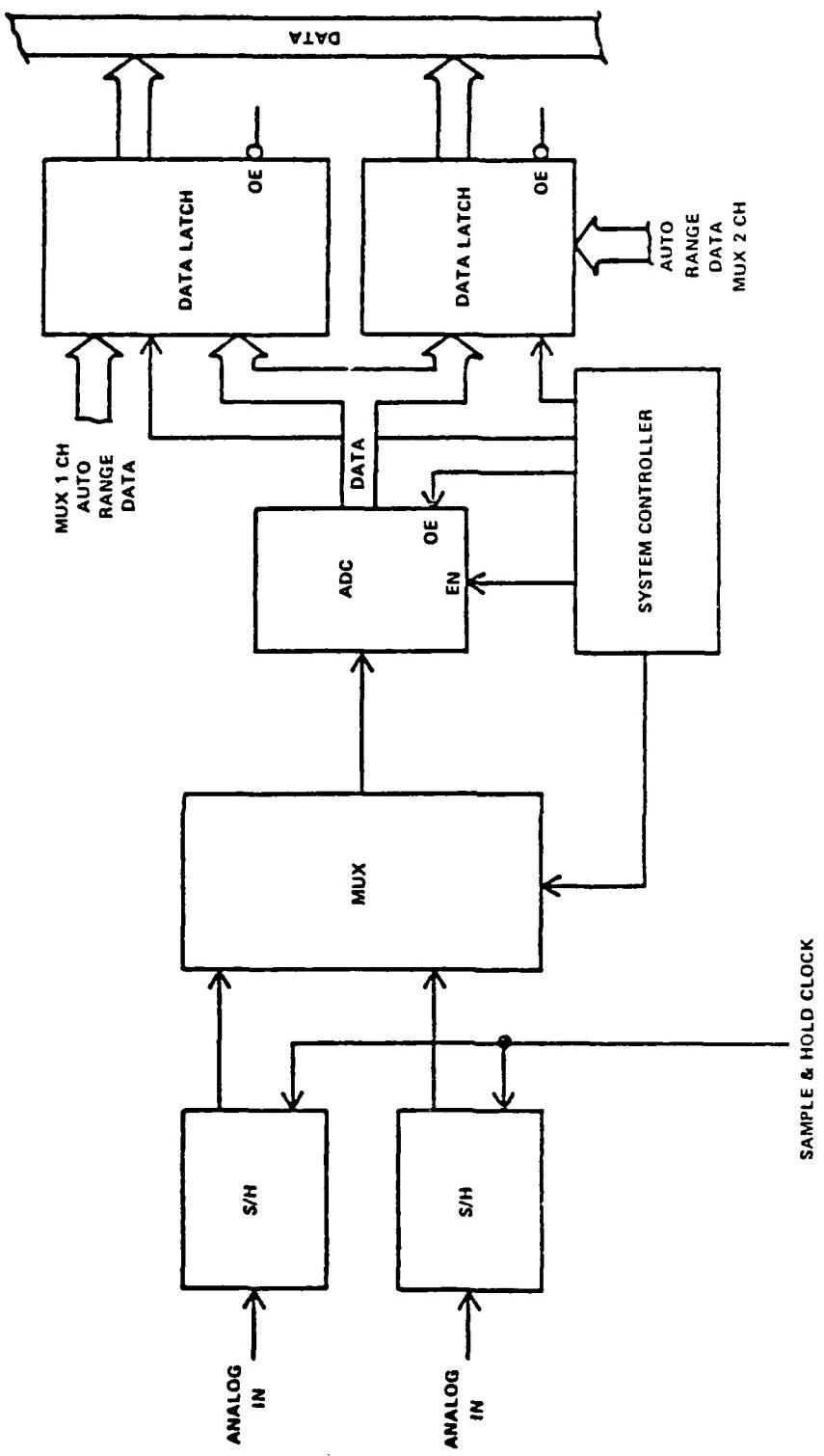


FIGURE C-22
MULTIPLEXED ADC

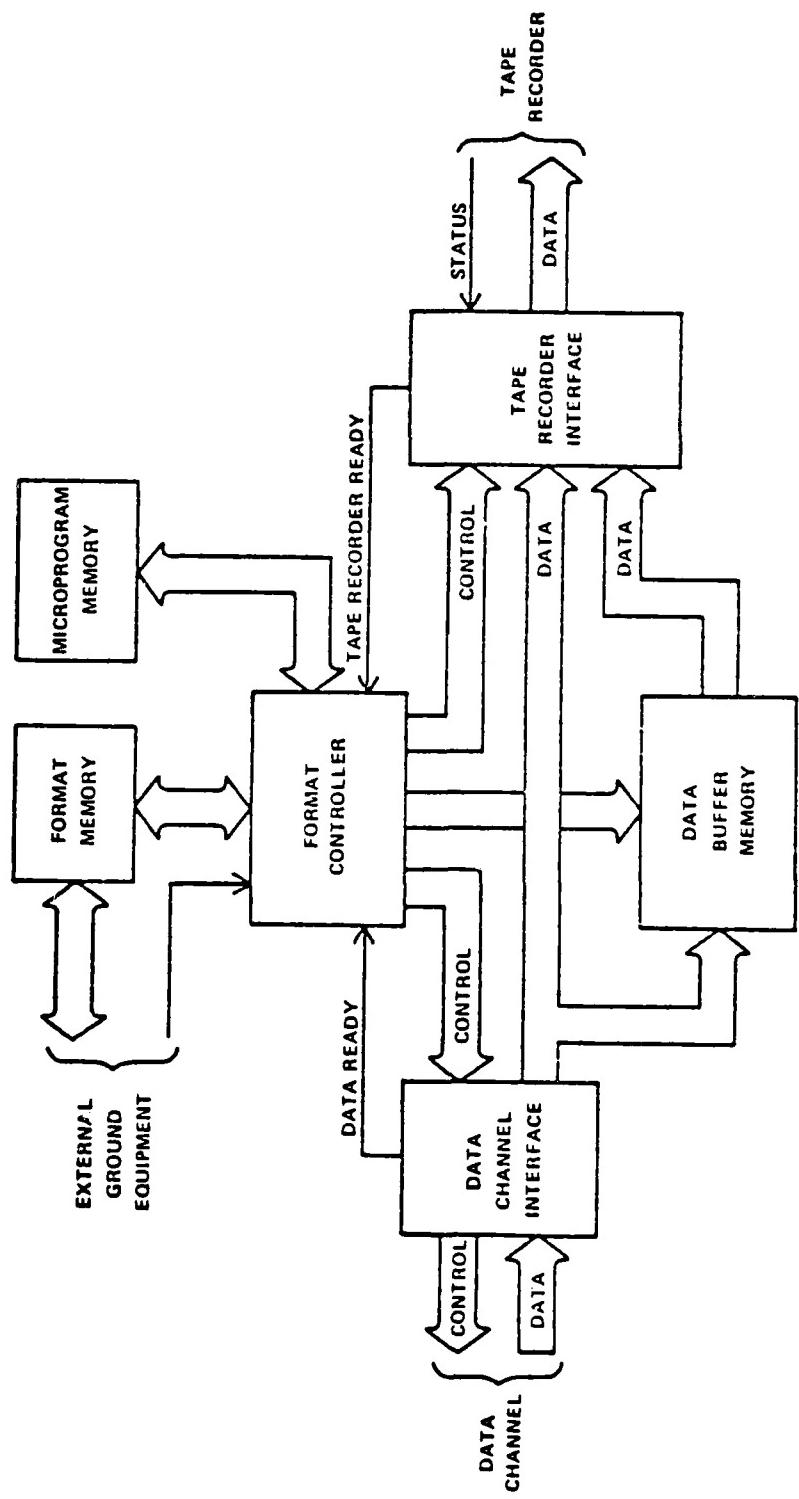


FIGURE C-23
DATA FORMATTER BLOCK DIAGRAM

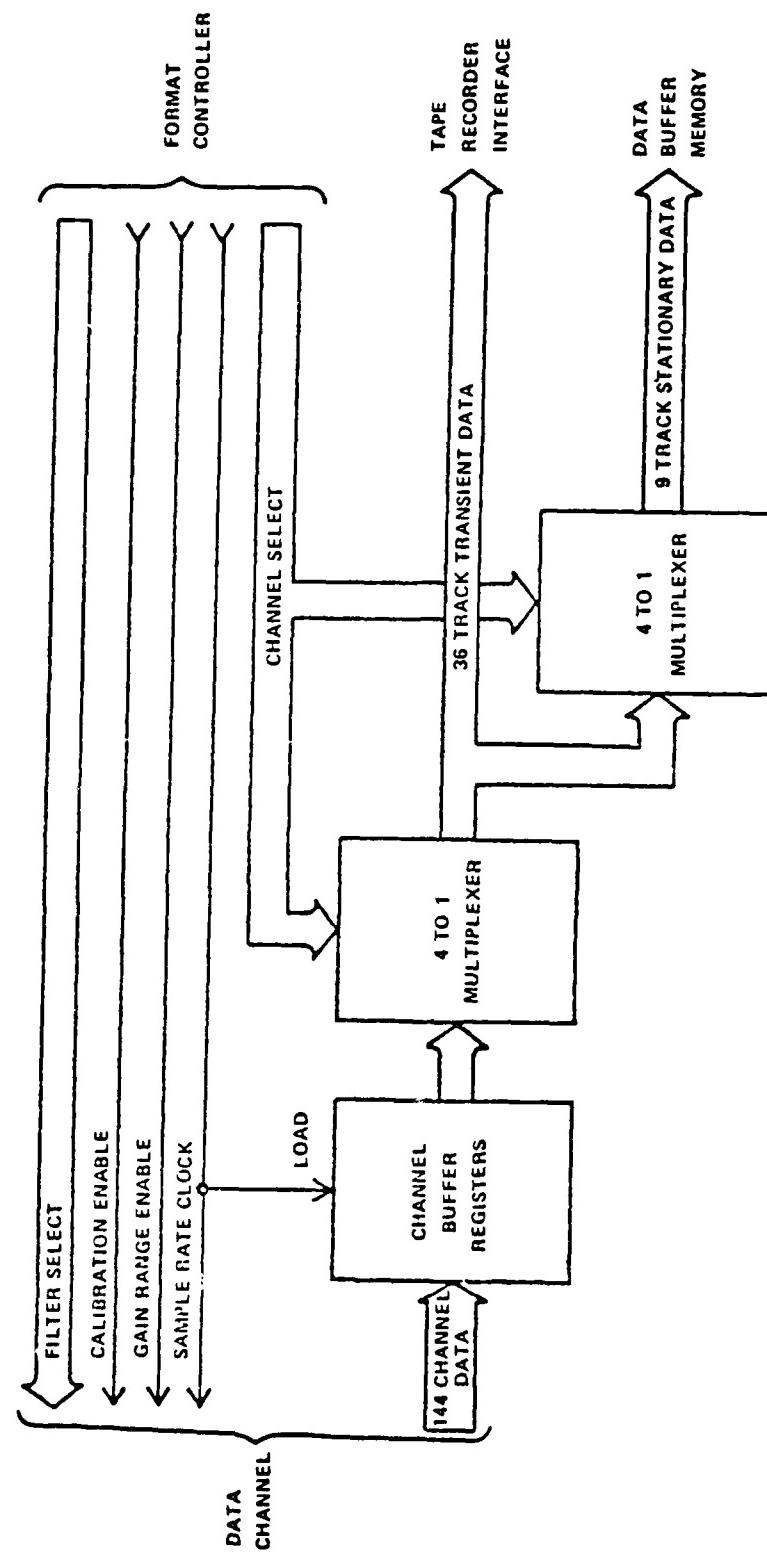


FIGURE C-24
DATA CHANNEL INTERFACE BLOCK DIAGRAM CENTRALIZED PCM SYSTEM

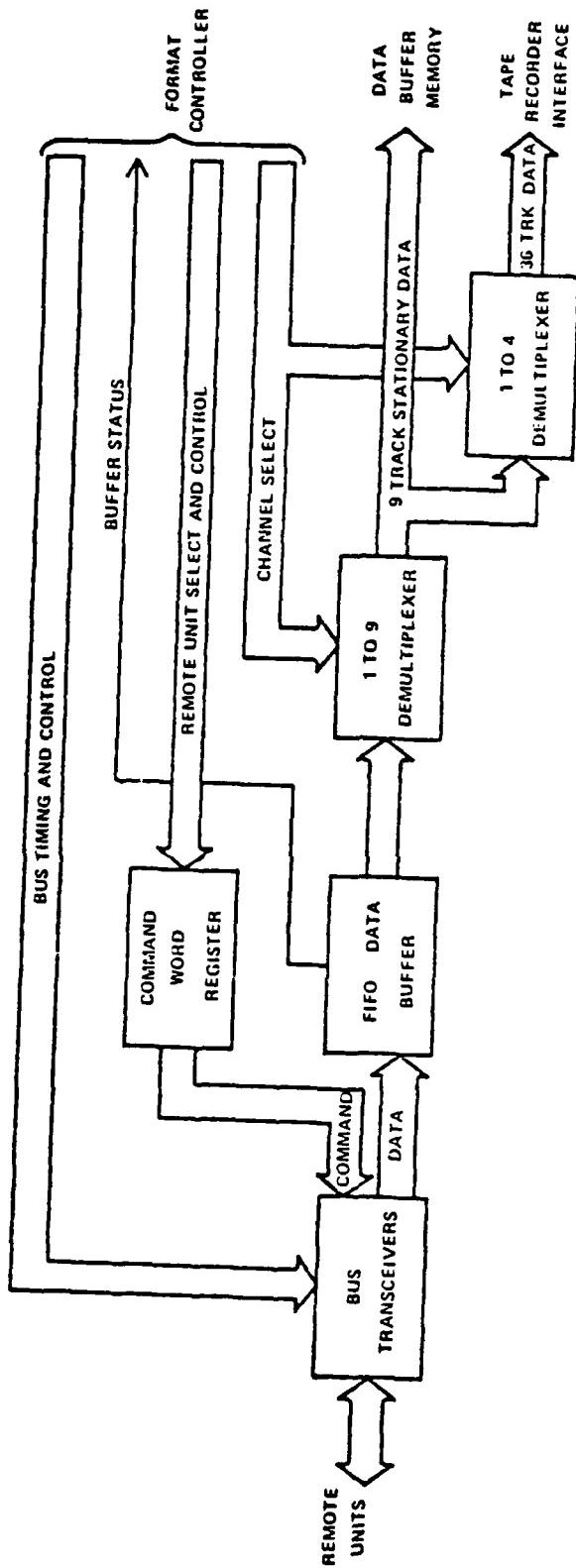


FIGURE C-25
DATA CHANNEL INTERFACE BLOCK DIAGRAM DISTRIBUTED PCM SYSTEM

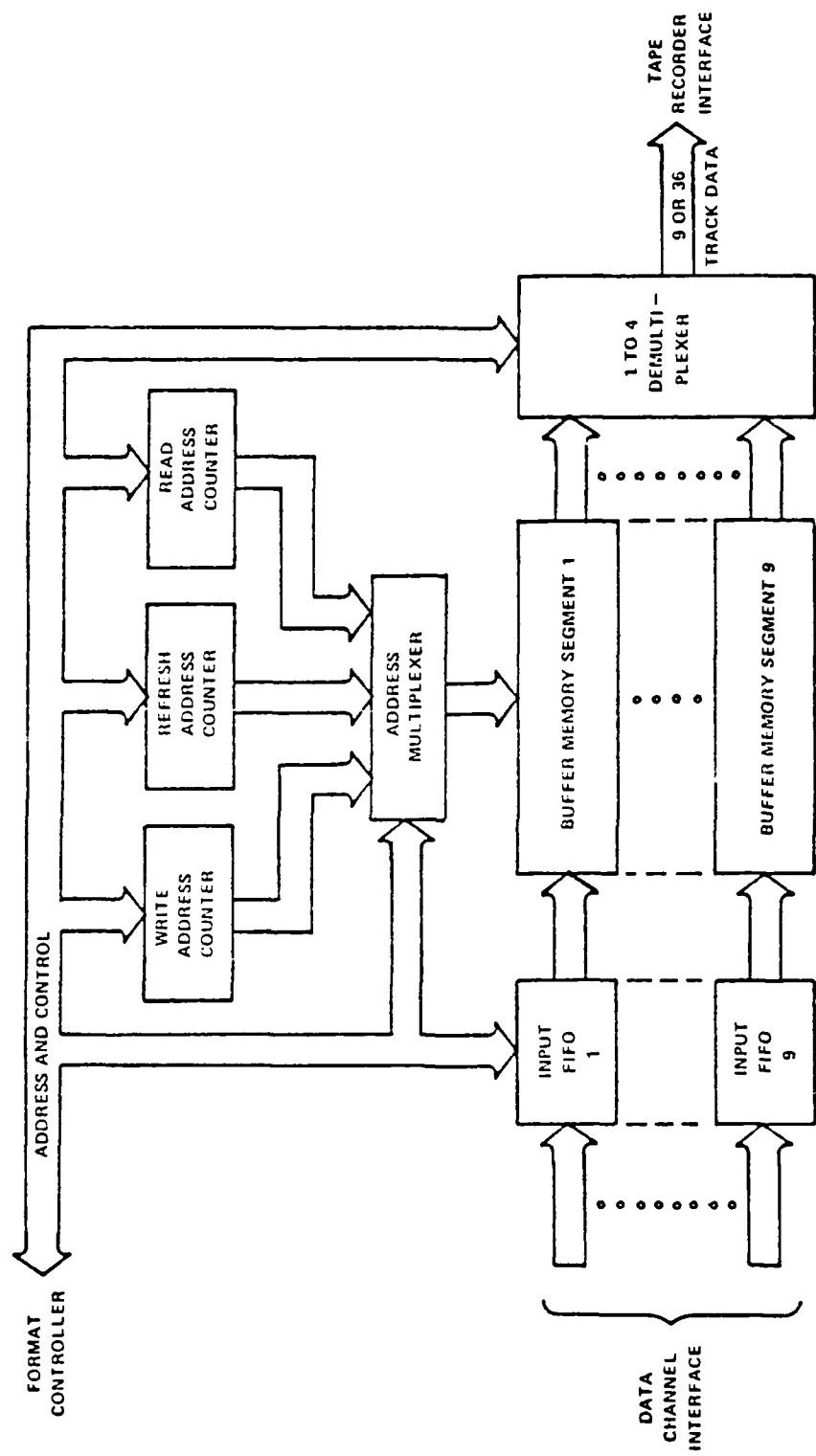


FIGURE U-26
DATA BUFFER MEMORY BLOCK DIAGRAM

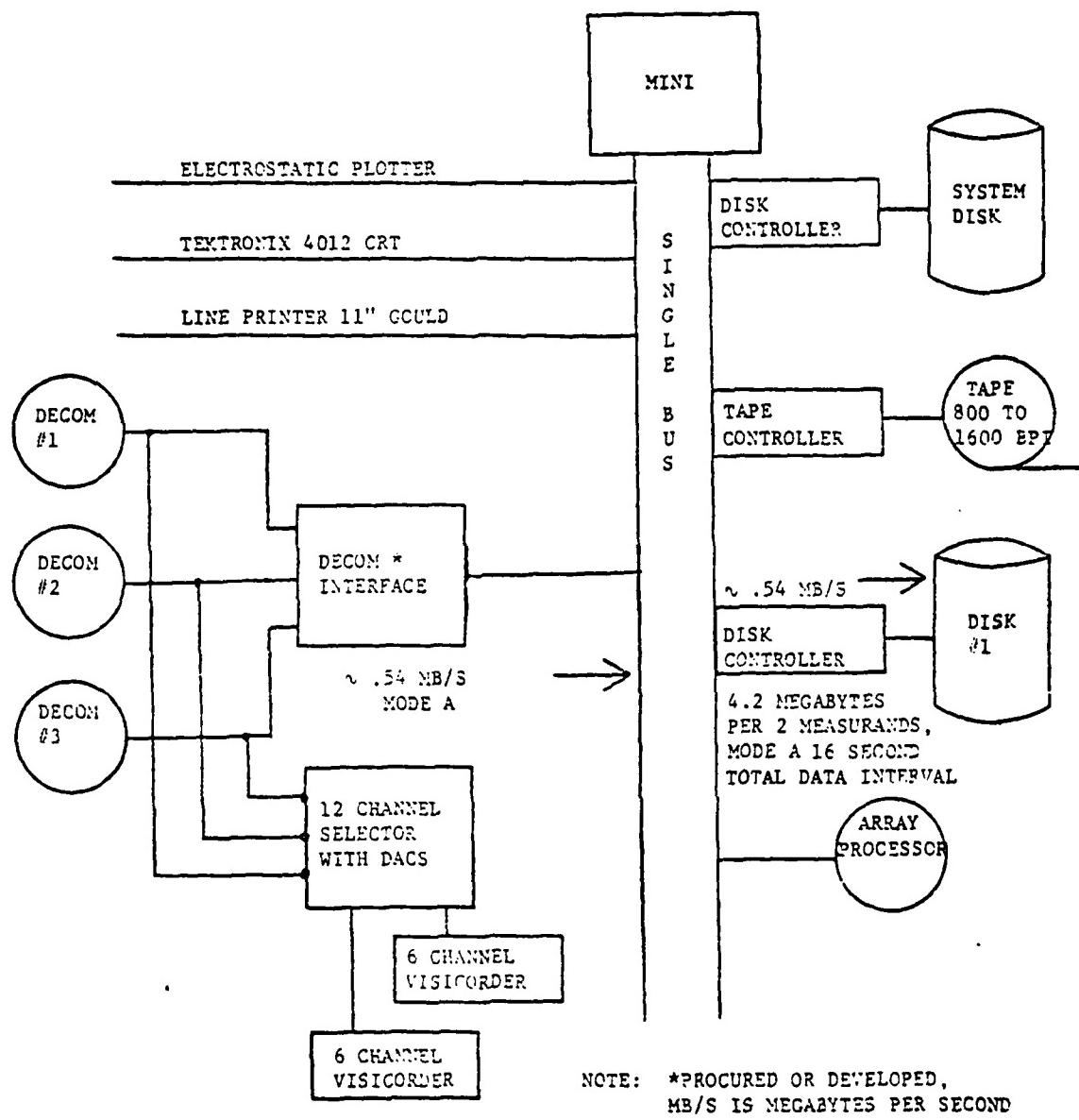
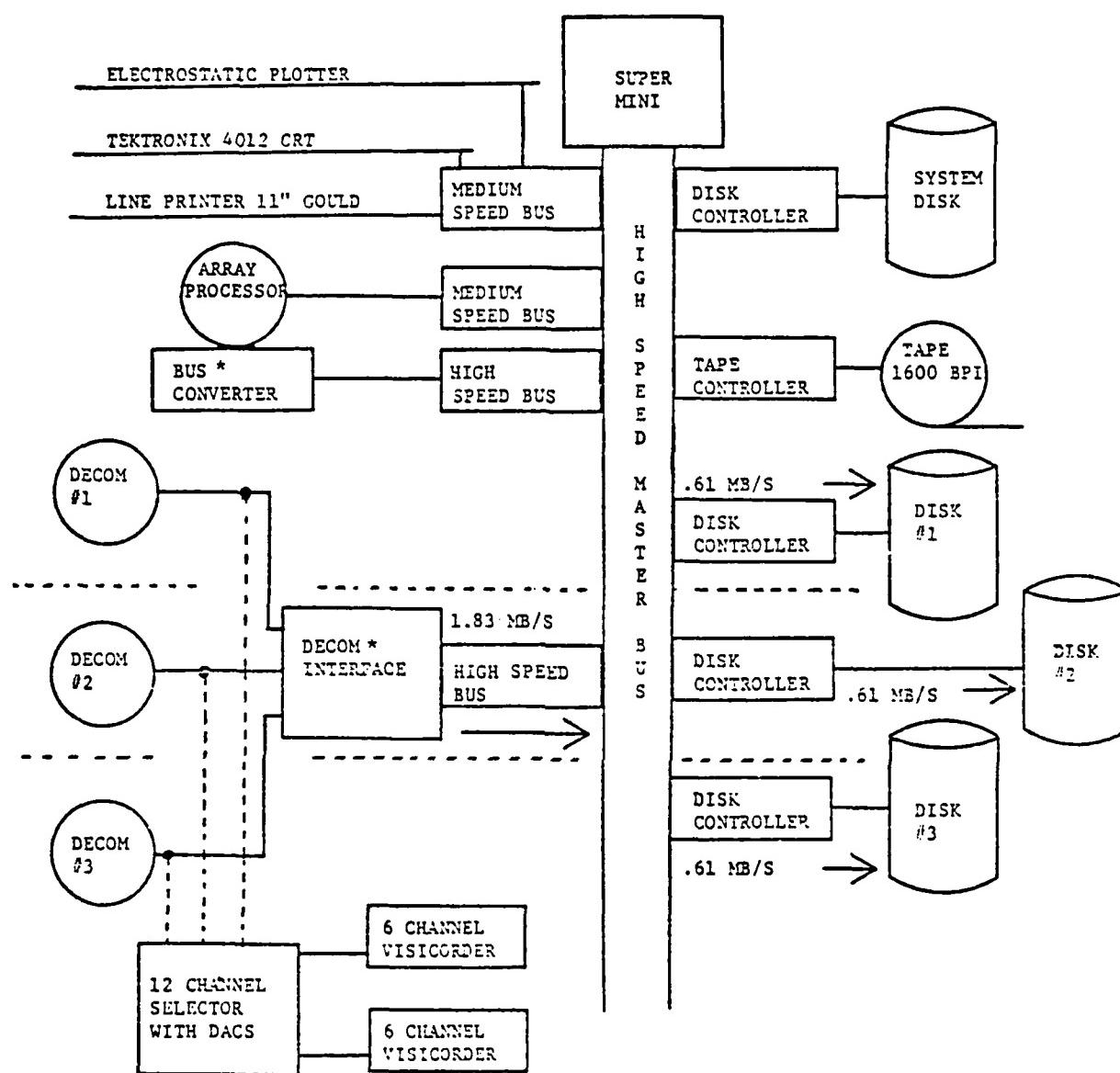


FIGURE C-27
ANALYSIS, EDIT, AND DISPLAY SYSTEM BASIC CANDIDATE



COMMENTS:

STEP 1 = EDIT

~ 800 MEGABYTES WILL BE REQUIRED TO STORE 100% OF THE TEST TAPE ON DISK FOR 12 MEASURANDS FROM MODE A.

STEP 2 = ANALYSIS

~ 25.2 MEGABYTES TOTAL DISTRIBUTED OVER THREE DISKS ARE NEEDED TO STORE ONE SINGLE 16 SECOND DATA INTERVAL FOR 12 MEASURANDS FROM MODE A.

NOTE:

* PROCURED OR DEVELOPED HARDWARE, NOT "OFF THE SHELF"

FIGURE C-28
ANALYSIS, EDIT, AND DISPLAY SYSTEM HIGH CAPACITY CANDIDATE

APPENDIX D
ADDENDUM NO. 1 TO
PHASE II INTERIM REPORT
APPLICATION OF PULSE CODE MODULATION (PCM)
TECHNOLOGY TO AIRCRAFT DYNAMICS DATA ACQUISITION

Revision date

Revision letter

Issue date 16 May 1980

Contract number F33615-79-C-3205

Prepared by



C. J. Guenther
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Approved by



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Program Manager

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1. INTRODUCTION

This report documents changes to results reported in Appendix C, "Phase II Interim Report, Application of Pulse Code Modulation (PCM) Technology to Aircraft Dynamics Data Acquisition". The changes identify the configurations to be studied during Phase III, and are based on AFWAL/FIBG directives following the Phase II Briefing.

2. SUMMARY

On 24 April 1980, the contract briefing for Phase II was held at AFWAL/FIBG.

During the briefing MCAIR together with its' subcontractor SCI Systems, Inc. summarized the candidate PCM systems described in the Phase II Interim Report (Reference 1). The overall PCM system desired by AFWAL/FIBG was divided into three subsystems with candidates offered for each as follows:

(a) Airborne PCM Encoder/Formatter System

Eight candidate systems were based on all possible combinations of the following three choices:

- ° System Architecture - Distributed or centralized.
- ° Analog to Digital Conversion Configuration - a dedicated A/D per measurand or a multiplexed A/D per two measurands.
- ° Filter Implementation - Four analog plus two digital filters, or four fixed frequency switched capacitor filters plus two digital filters.

(b) Tape Record/Reproducer System

Two candidate sets of characteristics were offered, based on serial recording using either a 28 track or 42 track head configuration.

(c) Ground System for Editing, Analysis and Display

Two candidates were presented - a "basic" system utilizing a minicomputer, and a "high-capacity" system based on a "super" minicomputer.

Subsequent to the 24 April Phase II Briefing, AFWAL/FIBG directed (Reference 2) MCAIR to:

- (1) Delete from consideration in Phase III the centralized architecture and the multiplexed A/D configuration in the airborne encoder/formatter.
- (2) Add a new multiple filter implementation scheme based on the use of two variable switched capacitor filters per measurand.

- (3) Delete from consideration in Phase III the 42 track head configuration in the record/reproduce system.
- (4) To study both the basic and high capacity ground systems in Phase III. The net effect of these changes is to identify three airborne encoder/ formatter system candidates, based on filter implementation:
 - ° Four analog + 2 digital filters per measurand.
 - ° Four fixed frequency switched capacitor filters + 2 digital filters per measurand.
 - ° Two variable switched capacitor filters per measurand.

Each of the three candidates has distributed architecture and a dedicated A/D converter per channel and uses a 28 tape track record/reproduce system.

3. AIRBORNE PCM ENCODER/FORMATTER SYSTEM CANDIDATES

3.1 DISTRIBUTED ARCHITECTURE

Although the centralized architecture features slightly less power, weight, and size, the distributed architecture was chosen for Phase III because of its greater degree of modularity and flexibility in setup. The distributed system affords a better chance of accommodating the component packages in available space in the test vehicle.

3.2 DEDICATED A/D CONVERTER PER MEASURAND

The dedicated A/D converter was chosen over the multiplexed configuration because of the greater likelihood of achieving the .5% goal for accuracy.

3.3 FILTER IMPLEMENTATION

A choice of two filter implementations for the selected multiple filter encoding configuration (six low-pass filters per measurand, with cutoffs two octaves apart) was presented in Reference "1" report. One utilizes four analog filters (active voltage controlled voltage source, VCVS) for the four highest cutoff frequencies, and time-shared finite impulse response (FIR) digital filters for the two lowest cutoff frequencies. (See Figure D-1.) The other implementation uses four fixed frequency switched-capacitor-filters (SCF's) for the four highest cutoff frequencies, plus the two FIR digital filters. (See Figure D-2.)

Due to the relative ease of changing cutoff frequencies of the switched capacitor filters (the cutoff frequency of a SCF is determined by its' sampling rate which is controlled by an input clock) an approach utilizing a single filter per measurand would appear to be very attractive in terms of reducing system size and power requirements. In this case a single filter would provide the functions of all six low-pass filters by switching through all the required cutoff frequencies in sequence. (Additional settling time would have to be

allowed due to transient response of the filter as its cutoff frequency is changed). An evaluation of this approach with currently available SCF's (Reticon R5609) indicates that, due to aliasing inherent in the SCF's, the single variable SCF would have to be preceded by a variable analog anti-alias filter (3 poles, minimum). This is undesirable due to the complexity involved in switching the analog filter. However, an approach using two variable SCF's (Figure D-3) may be workable with a fixed analog anti-alias filter. This latter approach appears to have the potential of minimizing power and size requirements, therefore it will be evaluated in Phase III along with the other two filter implementations.

The results of a preliminary evaluation of the three systems are shown in Table D-1. All goals are met or potentially achievable except for size, weight and power requirements.

7 POLE CHEBYSHEV
ANALOG FILTERS

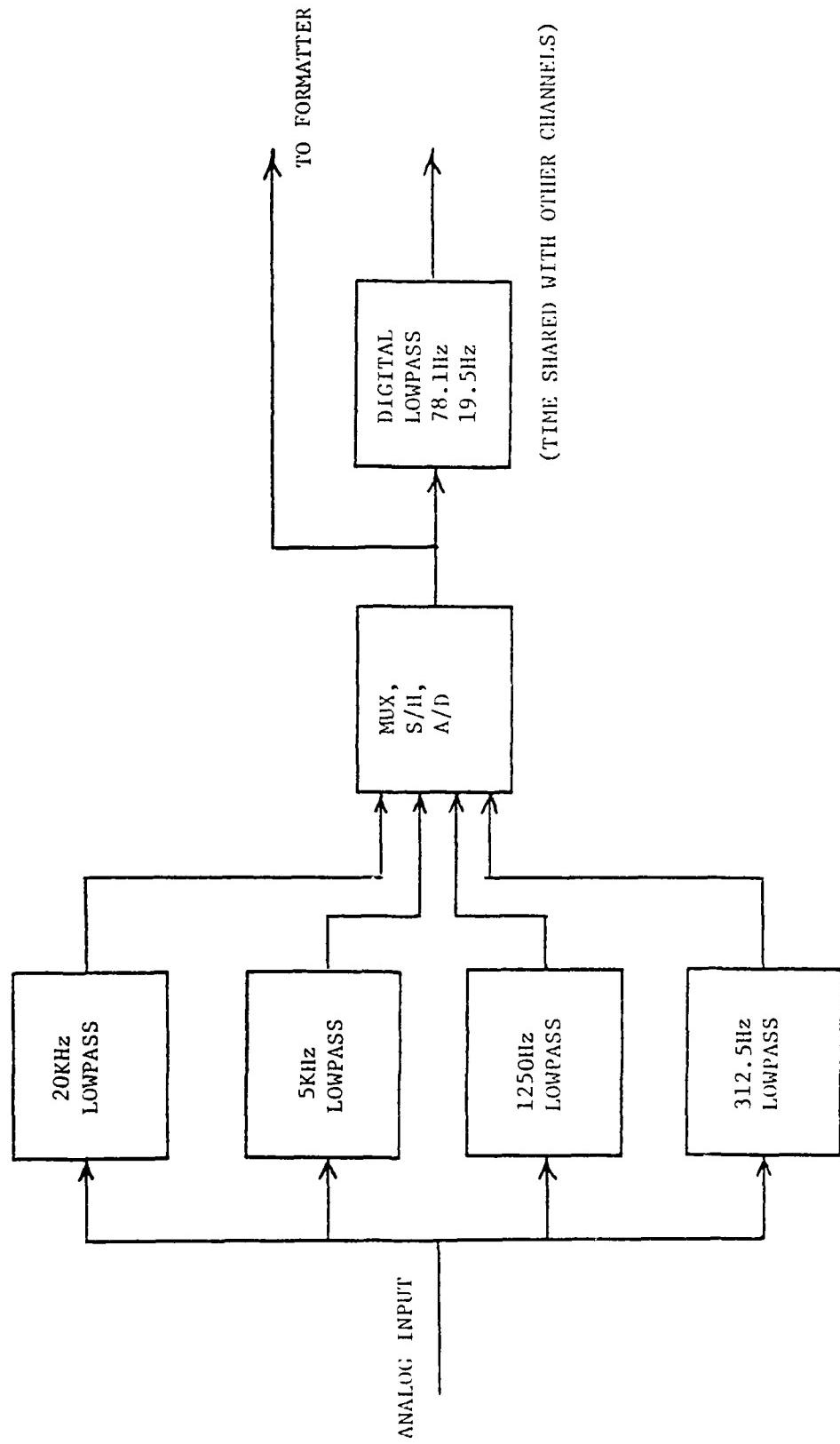


FIGURE D-1
FOUR VCVS ANALOG + TWO DIGITAL FILTERS

AD-A104 775

MCDONNELL AIRCRAFT CO ST LOUIS MO

F/G 14/2

APPLICATION OF PULSE CODE MODULATION (PCM) TECHNOLOGY TO AIRCRAFT—ETC(U)

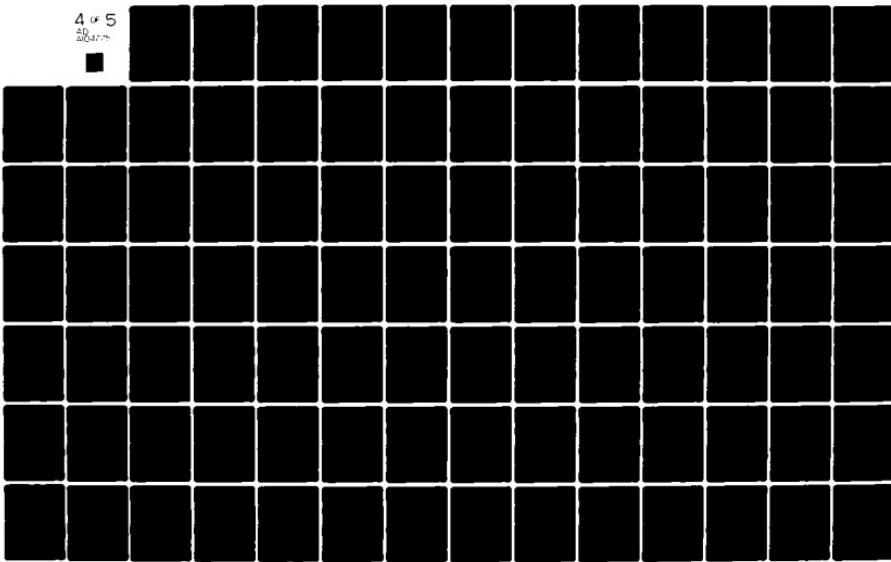
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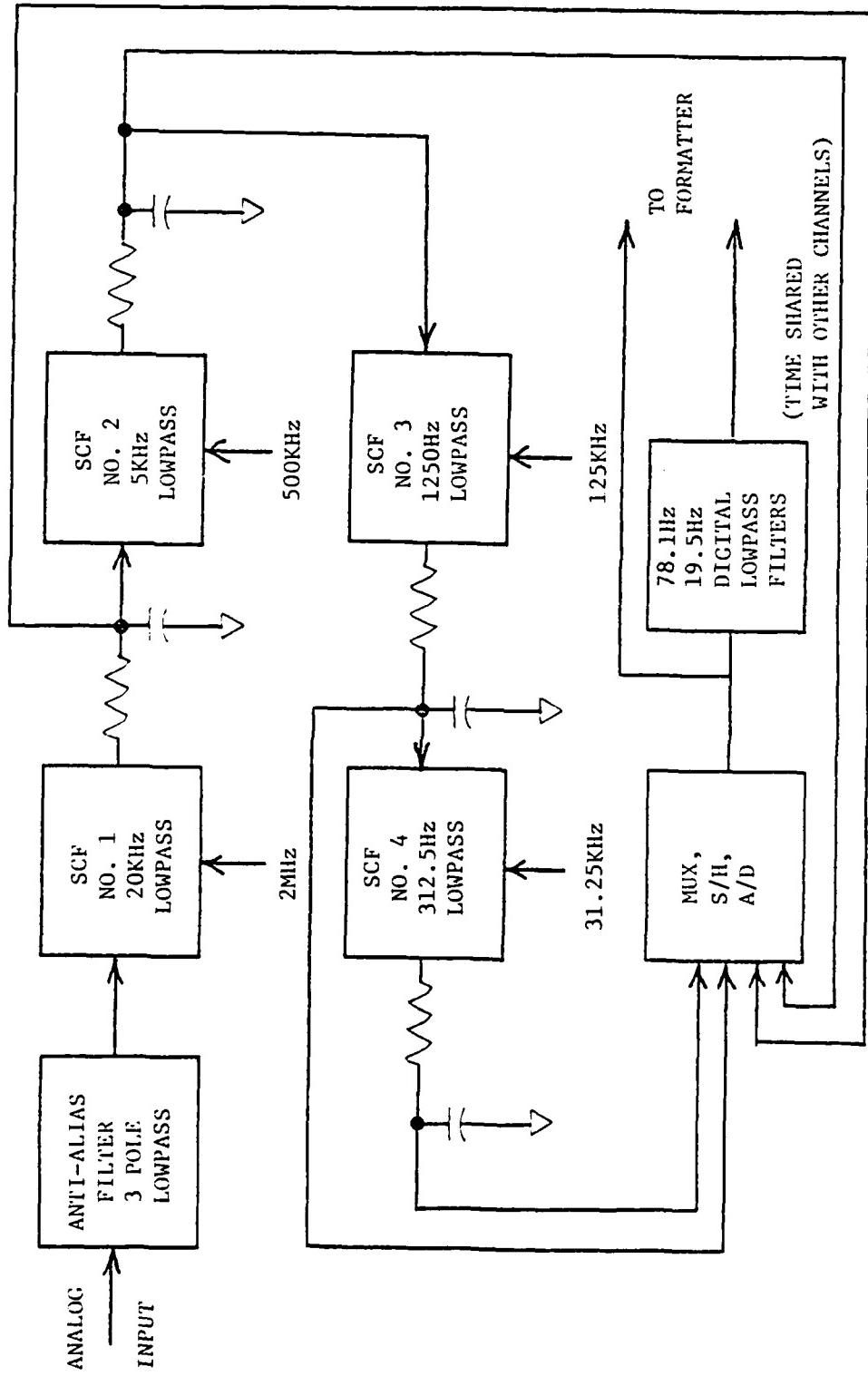
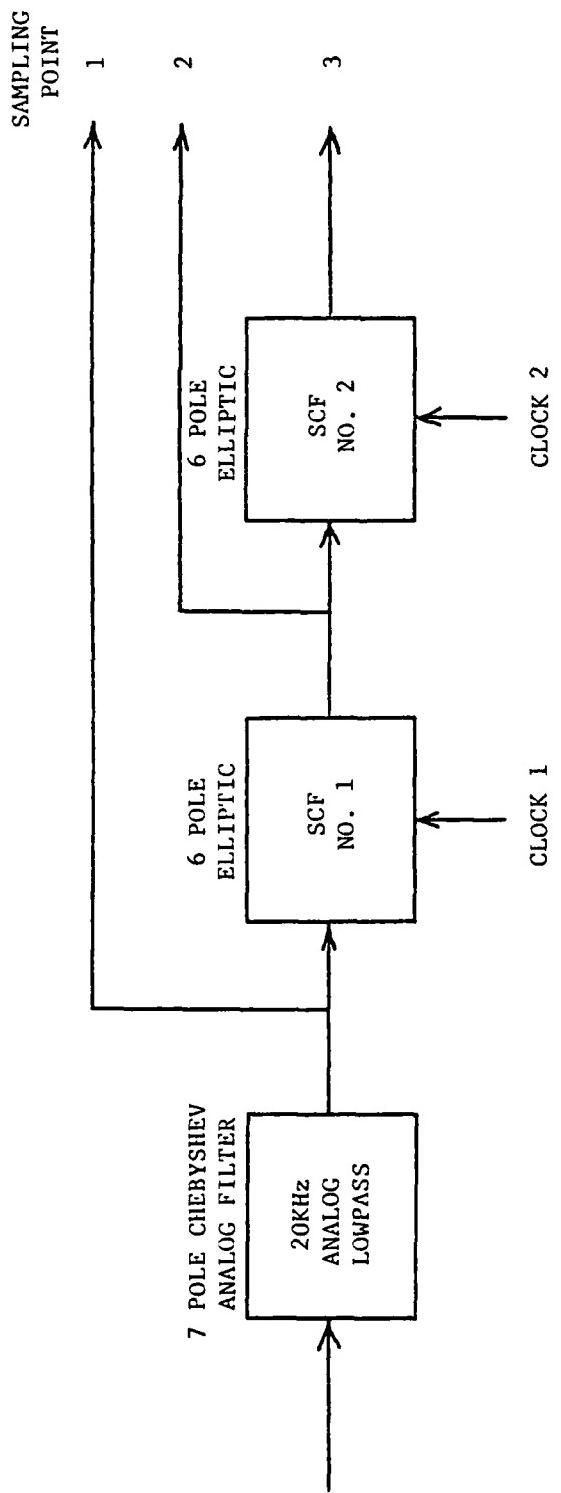


FIGURE D-2
FOUR SCF'S + TWO DIGITAL FILTERS



FILTER NO.	CUTOFF FREQ.	SAMPLING POINT	SCF NO. 1 CUTOFF	CLOCK	SCF NO. 2 CUTOFF	CLOCK
0	20 kHz	1	X	X	X	X
1	5 kHz	2	5 kHz	500 kHz	X	X
2	1250 Hz	3	5 kHz	500 kHz	1250 Hz	125 kHz
3	312.5Hz	3	1250 Hz	125 kHz	312.5Hz	31.25 kHz
4	78.1Hz	3	1250 Hz	125 kHz	78.1Hz	7812.5 Hz
5	19.5Hz	3	625 Hz	62.5 kHz	19.5Hz	1953.125Hz

X = DON'T CARE

FIGURE D-3
ONE VCVS ANALOG + TWO VARIABLE SCF'S

TABLE D-1
PHASE II CONCLUSIONS - AIRBORNE ACQUISITION SYSTEMS

CANDIDATE SYSTEMS CONFIGURATIONS BASED ON FILTER IMPLEMENTATION				
STANDARD	GOAL	4 VCVS + 2 D	4 SCF + 2 D	1 VCVS + 2 VARIABLE SCF
1. BANDWIDTH/MEASURAND	DC TO 20KHZ	Y	Y	Y
2. ACCURACY	.5%	P	P	P
3. ENCODING RESOLUTION	12 BITS PLUS 3 BITS AUTO-RANGE	Y	Y	Y
4. DYNAMIC RANGE	66 DB PLUS 70 DB AUTO-RANGE	Y	Y	Y
5. NUMBER OF MEASURANDS	144	Y	Y	Y
6. INTER-CHANNEL PHASE ERROR	5°	P	P	P
7. RECORD TIME	A) TRANSIENT B) STATIONARY	7.5 MINUTES 8.0 HOURS	(1) Y Y	(1) Y Y
8. PHYSICAL	A) SIZE B) WEIGHT C) MODULARITY	2.0 CUBIC FEET 50 POUNDS N.D.	6.0 319 3.49	6.0 319 3.49
9. ENVIRONMENTAL CONDITIONS	MIL E-5400, CLASS 2		Y	Y
10. POWER	112 WATTS @ 28 VDC		1520W.	1470W.
11. RELIABILITY	1000 HOURS		TBD	TBD
12. MAINTAINABILITY	N.D.		TBD	TBD
13. TEST READINESS	N.D.		TBD	TBD
14. CAPABILITY FOR ON-SITE EVAL.	ALWAYS		Y	Y
15. OPERATIONAL FLEXIBILITY	N.D.		TBD	TBD
16. RECURRING MANPOWER SUPPORT	N.D.		TBD	TBD
17. SYSTEM HARDWARE COSTS	N.D.		TBD	TBD

Y = YES, GOAL ACHIEVED; P = POTENTIALLY FEASIBLE; TBD = TO BE DETERMINED; N.D. = NOT DECLARED;

(1) ASSUMED A SINGLE TAPE RECORDER WITH 28 TRACKS @ 120 IPS AND 10 1/2 INCH REEL SIZE (72 MEASURANDS-TRANSIENT). TWO SUCH RECORDERS WOULD BE REQUIRED FOR 144 MEASURANDS.

4. TAPE RECORD/REPRODUCE SYSTEM CHARACTERISTICS

Because of IRIG limitations for tape recorders, only the 28-track head configuration will be considered in Phase III.

5. GROUND EDIT, ANALYSIS AND DISPLAY SYSTEM CANDIDATES

The candidates for the ground system are unchanged as a result of the Phase II Review, and remain as reported in Reference 1.

REFERENCES

1. Appendix C, Phase II Interim Report, 28 April 1980.
2. Telecon D. Brown, AFWAL/FIBG: C. Detmer MCAIR, 6 May 1980.

APPENDIX E

PHASE III INTERIM REPORT

APPLICATION OF PULSE CODE MODULATION (PCM)

TECHNOLOGY TO AIRCRAFT DYNAMICS DATA ACQUISITION

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1. INTRODUCTION

This Interim Report is being submitted in compliance with Contract Data Requirements List (CDRL) Sequence Number 3 of Attachment Number 1 to Contract F33615-79-C-3205. It covers the contractor's (McDonnell Aircraft Company) work on Phase III (PCM Systems Evaluation) of the study authorized by this contract.

1.1 OVERALL STUDY OBJECTIVES

The objectives of this study are to provide AFWAL/FIBG with the following:

- (a) The design of an optimum Pulse Code Modulation (PCM) data acquisition, playback, and analysis system utilizing all, part, or none of the present facility equipment, and
- (b) knowledge of the rationale, considerations, and judgements involved in the creation of that design.

The study involves four phases of effort as follows:

Phase I - Facility Review, Literature Search, Formulation of System Standards and System Goals

Phase II - Definition of PCM Systems

Phase III - Evaluation of PCM Systems

Phase IV - PCM System Design

The results of each phase must be approved by AFWAL/FIBG prior to starting work on the next phase.

1.2 PHASE III OBJECTIVES

- (a) Evaluate the candidate airborne and ground systems defined in Phase II per the system standards established in Phase I.
- (b) Perform trade-off studies in selected areas to indicate variations in cost and performance so that the optimum configuration can be defined in Phase IV.

1.3 REVIEW OF CANDIDATE SYSTEMS

Based on the results of Phase II (References 1 and 2), there are three candidate airborne encoder/formatter systems and two candidates each for the tape recorder/reproducer and the ground edit, analysis and display system. (The relationship of these systems within the overall PCM system desired by AFWAL/FIBG is indicated in Figure E-1.

The airborne encoder/formatter candidates all feature distributed architecture (remote encoding concept) and a dedicated (rather than multiplexed) A/D converter for each measurand channel. The candidates differ in their implementation of the multiple-filter encoding method (described in Reference 1). The primary operating modes (those featuring 20 KHz response) of the multiple filter encoding setup are summarized in Table E-1. The three candidate filter implementations are shown in Figures E-2, E-3 and E-4. System 1 uses four conventional active analog filters per measurand, located in the remote encoding unit, and a time-shared digital filter system in the control unit, to effectively provide six low-pass filters per measurand. System 2 is similar to System 1 except that the remote unit contains four switched-capacitor analog low pass filters per measurand instead of the conventional analog filters. The control unit for System 2 is the same as for System 1. System 3 accomplishes the required six filter functions with two tuneable switched capacitor filters per measurand in the remote unit. Thus, in this system, digital filters are not employed in the control unit.

The candidates for the tape recorder/reproducer are based on available reel sizes and tape speed ranges. Both candidates utilize serial high density digital recording with randomized NRZ-L code. As indicated in Table E-2, the only candidate that can currently be realized (for an airborne system) is the "state-of-the-art" candidate employing two recorders. This will require 48

tape outputs from the central control unit of the encoder/formatter system. If and when a 240 ips/14 inch reel airborne recorder becomes available, only one recorder will be needed to satisfy the goals, with only 24 tape outputs from the formatter.

Phase II studies resulted in a basic and a high capacity candidate for the ground edit analysis and display system (Figures E-5 and E-6). Both candidates achieve all goals with respect to standards for encoding resolution, maximum array size, computer precision, edit capability, plotter thruput, resolution, plotter software, and analysis software. The major difference between the basic and high capacity candidate is the higher thruput potential of the high capacity candidate.

1.4 COST DISCLAIMER

This report contains cost information for various systems and components. In all cases, this information should be considered as approximate; it is furnished as engineering evaluation reference for budgetary and planning purposes only. This report should not be construed as an offer by MCAIR or its subcontractor SCI Systems, Inc., or other suppliers to supply the equipment and services described.

2. SUMMARY OF CONCLUSIONS

2.1 AIRBORNE SYSTEM

The evaluation in Section 3 indicates that PCM encoder/formatter System 1 employing conventional analog filters is far more accurate than either System 2 or 3, and is somewhat more reliable and uses less power than System 2. System 3 contains a serious deficiency in aliasing rejection when Mode B (see Table E-1) is considered. In addition, the reliability of the switched-capacitor filters (used in Systems 2 and 3) is a problem, as discussed in Section 3.5. The latter two problems could be solved by improvements in switched-capacitor filters, however, at the present time, System 1 is the choice which most closely fulfills the goals.

2.2 GROUND SYSTEM - EDIT, ANALYSIS, AND DISPLAY

From the trade studies in Section 6.0, it is clear that no 16 bit host computer architectures and basic array processors can maintain the current mode of operation at AFWAL/FIBG with either 60 or 144 channels of data. A basic system cannot cope with either a typical 60-channel or worst-case 144 channel test setup.

A combined host computer and array processor system performance index of at least 7.7 is required for the typical 60 channel test set up. A combined system performance index of at least 9.24 is required for the worst-case or 144 channels. Since 144 channels is a goal from Phase I and based on AFWAL/FIBG input (Reference 3), the only conclusion is that a Floating Point System's AP-120B, which is faster and cheaper than a similarly configured CSP, Inc., Map 300, must be configured with a host computer which attains a combined performance index of 9.24. Host computers that meet this criteria are DEC VAX 11/780 VA and VB, Perkin Elmer (Interdata) 3240 VA and VB, Harris 800 VB and VC, Modcomp 870 VB, Prime 750 VB, Data General NV/8000 VB, and SEL 32/7780 VB and VC

(Reference Figure E-18).

All the previous systems, which include the AP-120B array processor, range in price for Version A systems from \$450,995 to \$511,750. Version B systems range in price from \$528,395 to \$639,695. Version A systems have disk capacities of 268 to 384 megabytes. This has been evaluated to be insufficient for AFWAL/FIBG applications. Version B and C will provide for smooth operations with minimal human intervention while maintaining nominally the same utilization of facility. Although disk storage space is not a Phase I standard, Version B provides from 835 to 1,447 megabytes. Also, except for Perkin Elmer, Modcomp and SEL (which do not employ virtual storage), any virtual storage operating system will run at a higher efficiency level in a 2 megabyte physical memory configuration than in 1 MB. (Version A only provides 1 megabyte.)

If AFWAL/FIBG is linked in any kind of a multi-user or network environment Modcomp, SEL, and Perkin Elmer should be eliminated because of their non-virtual operating systems. Prime in a multi-user or network environment should also be eliminated because of its slower MOPS CPU (see Table E-38). This leaves DEC VAX 11/780, Harris 800 and Data General MV/8000 as candidates. The latter two candidates were introduced to the market within the last year while the VAX 11/780 was introduced in 1978. Although all are in the same performance class the VAX 11/780 has achieved product maturity in hardware and software simply from its early market entry. Should the system be employed in a network environment it is concluded by MCAIR that the DEC VAX 11/780 is the recommended system for AFWAL/FIBG applications and network support for multi-users.

3. SYSTEMS EVALUATION - AIRBORNE

A summary of the evaluation of the three airborne encoder/formatter candidates combined with the airborne recorder is shown in Table E-3. This evaluation is with respect to the system standards and goals established in Phase I. Block diagrams of the encoder/formatter and recorder systems are shown in Figures E-7 and E-8, respectively. Within the encoder/formatter remote unit, the three candidates differ in their implementation of the analog lowpass filters. System 1 uses conventional analog (VCVS) filters, while Systems 2 and 3 both employ newly developed "switched-capacitor" filters (SCF). The control unit for Systems 1 and 2 is the same - it includes the digital filter system indicated in Figure E-7. The control unit for System 3 does not use digital filters. The tape recorder interface in the control unit requires 48 tape outputs using the current state-of-the-art tape recorder; however, with the "future" tape recorder candidate only 24 tape outputs will be needed.

The evaluation summarized in Table E-3 was based on encoder/formatter system design information furnished by MCAIR's subcontractor, SCI Systems, Inc., and vendor specifications for the Sangamo Sabre XII airborne recorder. Systems 2 and 3 are based on the use of Reticon R5609 switched-capacitor low-pass filters. Since the vendor specifications on the R5609 were incomplete, the system evaluation is based, in part, upon MCAIR test results on this component, as reported in the Addendum.

System 1 is based on the characteristics of 7-pole Chebyshev filters with 0.1 dB (peak-to-peak) passband ripple. For System 2, a 3 pole passive anti-alias filter (40 KHz Butterworth) was assumed in front of the four cascaded SCF's (reference Figure E-3). For System 3, a 7-pole Chebyshev low-pass filter (.1 dB ripple) was assumed in front of the two variable SCF's (reference Figure E-4).

3.1 ERROR ANALYSIS

An error analysis was performed in order to compare frequency response errors, DC accuracy, dynamic range, and inter-channel phase error, for the three systems. A summary of results is shown in Table E-5 with the contributions from the various system components detailed in Table E-6.

System 3 immediately stands out as having insufficient aliasing attenuation, thus limiting dynamic range to only 38 dB. An analysis of the aliasing protection using this filtering approach indicates that this problem could be solved by:

- (1) using a sharper analog anti-alias filter (at least a seventh-order elliptic) and
- (2) using SCF's that have either higher internal sample rates or sharper filter characteristics (higher transition ratio) than the R5609.

Figure E-9 indicates a locus of SCF characteristics (sample rate versus transition ratio) required for both multiple filter modes B and C. Note that the theoretical performance of the R5609 (seventh-order elliptic) would suffice for both modes; however the measured performance falls short of being adequate for Mode B.

The best DC accuracy is exhibited by System 1, although it falls short of the goal of 0.5%. The major error contributor in System 1 is offset error in the AGR amplifier.

Table E-5 indicates that Systems 2 and 3 may not meet the goal for inter-channel phase error, while System 1 can if initial phase errors are adjusted out during manufacture of the VCVS analog filters.

3.2 POWER ANALYSIS

Tables E-7 and E-8 summarize the estimated power requirements for a control unit and a 16 channel remote unit, respectively. Table E-9 indicates the

remote unit power dissipation for System 1 with 8, 12, or 16 channels per remote unit. These power numbers were used to calculate the total power requirements shown in Tables E-3 and E-4, and as input to the thermal analysis.

3.3 PACKAGING CONSIDERATIONS

The Control Unit and Remote Unit are packaged with thermally identical constructions that have the same external size and geometry. A package size of 9.75" X 9.25" X 8.38" is used. All internal electronic components are mounted on metallic heat strips and specific heat sinks to provide a high degree of heat conduction from the component bodies through bonded joints to the main housing outer surface.

Except for the power supply module, all of the PC modules are constructed using a .050 inch thick copper heat strip overlay laminated to the .062 inch multilayer PC board. The heat strip overlay covers the 9.00 X 6.9-inch usable board area which allows for up to 14 strip rows .200 inches wide by 8.25 inches long connected to .375 inch wide border strips on each 6.9 inch board end. The .200 inch wide strip provides a heat sink for the 14 - 16 DIP package parts which straddle-mount the strips and are thermally secured through a bonded joint on the component body bottom (see Figure E-11). Other parts types, such as the 1.0 X 1.5 inch hybrid parts, will have specific mounting provisions tailored for their particular mounting requirements on the heat plane overlay. In addition, these higher-powered parts will be located near the PC module mounting edges to keep their conductive heat path length as short as possible.

The PC logic modules are secured to the main housing walls through metallic PC card guides such as the Birtcher zero-insertion force devices which have lever cams to provide good thermal clamping after module insertion. These card guides are bonded to the housing inner wall surfaces to further enhance the thermal conduction between the two opposite 6.9-inch PC module edges and

the main housing.

3.4 THERMAL ANALYSIS

The external surfaces of the 9.75 X 9.25 X 8.38 inch main unit housings are the heat transfer mechanisms which passively transfer the internally generated heat power to ambient by radiation and free-air convection. The flat-sided surface area of the main housing is about 498.8 square inches. In order to enhance the free-air convection mode, the housings are constructed with short fins measuring about .062 inches thick by .5 inches tall and with spacings between adjacent fin sides ("groove" widths) of about .395 inches. Keeping the fin tips within the 9.75 X 9.25 X 8.38 inch envelope, this allows for 20 fins and about 275.2 square inches of total area on each of the "top" and "bottom" 9.75 X 9.25 inch surfaces, and 70 fins and 934.4 square inches on the 8.38 inch housing "sides".

Since fins act to restrict the free air flow as compared to actual flat planes, the effective convection area gain is approximately 80% of the total area gains.

Figure E-12 indicates for two different ambient temperatures (including the 71°C worst-case steady-state environment of MIL-E-5400 Class 2) the calculated remote unit housing temperature versus power dissipation within the remote unit.

Figure E-13 is a plot of the remote unit housing temperature versus ambient temperature. Also indicated are the worst-case DIP junction temperature (98.92°C) and the hybrid A/D junction temperature (106.1°C) calculated at the 71°C ambient, sea level condition.

Figure E-14 shows the results of a similar analysis on the central unit. The housing temperature with and without the fins is shown for comparison.

It is concluded that the PCM remote unit and control unit have the potential of meeting the MIL-E-5400 Class 2 environment.

However, the tape recorder does not meet the environmental requirements (-55°C) at the low temperature end. The Sabre XII is specified to operate down to -20°C (or down to -40°C with an optional heater).

3.5 RELIABILITY ANALYSIS

Reliability calculations for the three encoder/formatter systems are summarized in Table E-10. Failure rates were derived from MIL-HDBK-217C, with assumptions as follows:

- ° Ambient Temperature: 57°C
- ° Airborne Inhabited Transport Environment
- ° Parts Quality Levels:

IC's: Class B

Semiconductor: TX

Passive Parts: ER Level P

It should be noted that the SCF's currently available (Reticon R5609) are commercial parts and hence Quality Level D per MIL-HDBK-217C, with a failure rate 75 times that of Class B. The resultant MTBF's for Systems 2 and 3 with currently available SCF's then, are only 41 hours and 59 hours, respectively. Clearly these MTBF's are dominated by the SCF failure rates. Thus, it is concluded that currently available SCF's will result in unsatisfactory reliability of Systems 2 and 3, and that these parts need to be upgraded to Class B quality level.

3.6 TEST READINESS AND OPERATIONAL FLEXIBILITY

The test readiness capabilities of the airborne PCM system include a pre-flight test interface for verification of overall system data throughput integrity, and a portable format memory programmer for on-site programming of the data sampling formats required for the various phases of an aircraft flight test program.

The PCM system provides a serial PCM output port for pre-flight quick-look data verification. The test data may be a fixed known signal applied to all data channels or the instrumentation transducers of the aircraft. Data source selection is provided by an externally controlled input multiplexer at each data channel input. The multiplexer is utilized for both pre-flight readiness tests and system calibration.

An additional externally controlled multiplexer is provided at the serial PCM output port to minimize the cabling required for pre-flight test functions. This multiplexer selects one of the multi-track tape recorder outputs for quick-look data verification. The serial PCM output is supplied to a PCM de-commutator for data channel display and verification.

The format memory programmer is a compact, microprocessor controlled unit with a CRT terminal and tape cassette playback interface for programming flight test formats. The PCM system format memory is implemented with ultraviolet-erasable PROM's packaged in a removable module on the airborne data formatter for fast turnaround data format programming. The module is inserted into the memory programmer for one of several modes of format programming. The existing format may be stored in the programmer memory, modified via the CRT terminal, and reloaded into the format memory. New formats stored on tape cassettes may be selected for programming of the format memory. The tape cassette interface provides an inexpensive means of transporting data sampling formats from a central flight test facility to remote on-site flight test programs.

3.7 MAINTAINABILITY AND RECURRING SUPPORT

Since the analog filtering represents a relatively small portion of the remote unit, there would be little, if any, difference in maintainability and recurring support among the three candidates remote units. Maintainability of System 3's control unit would be superior to both System 1 and 2, however,

because it does not employ the digital filter.

4. SYSTEMS EVALUATION - GROUND EDIT, ANALYSIS, DISPLAY

4.1 INTRODUCTION

The major thrusts of Phase III studies have been twofold for the ground system. First, the minimum performance criteria has been formulated for average and worst case loading of any proposed ground system. Second, 12 basic candidate ground systems and 19 high capacity candidate ground systems have been uniformly analyzed by a common performance model.

The results from the first effort answered what workload level the current Raytheon 704 host computer with an Array Transform Processor was handling in the current AFWAL/FIBG PCM Data System. In Reference 3 telecon, the following information was obtained regarding usage of AFWAL/FIBG's airborne data system and their ground computer facility:

- (A) Usage of the 704 averages out to roughly four hours per working day.
- (B) Approximately 75% of test flights have utilized more than 12 data channels (by stepper switching of the existing twelve channel FM system).
- (C) A typical requirement would be for 60 data channels (with a new system). Based on Raytheon utilization, average and worst case loading estimates were obtained for any proposed ground system in relative terms to the existing Raytheon 704 system. These estimates establish what will be required minimally by any proposed ground system to keep up with the projected increased workload from a new PCM system.

The results from the second effort gave answers as to how a high capacity candidate will differ in performance relative to a basic candidate and how either basic or high capacity candidates perform in relative terms to the Raytheon 704 system. To achieve this, detailed configuration information involving model numbers, quantities, descriptions, and prices were developed for 31 different ground system possibilities. In addition, a performance model was

developed as the key tool for all Phase III ground system studies (see Tables E-22 and E-32).

Figures E-5 and E-6 remain the same, respectively, for both basic and high capacity candidate systems. All configuration efforts with Digital Equipment Corporation, Data General, Hewlett Packard, Perkin Elmer (Interdata), Harris, Modcomp, Prime, and Systems Engineering Laboratories were guided by these figures. Figure E-17 described an edit option on the high capacity Figure E-6. The advantage is that signal data could flow directly into the Array Processor, freeing more of the high capacity host for analysis or network processing.

4.2 STANDARDS AND GOALS

As previously mentioned in Section 1.3, all candidates, including the basic and high capacity systems, achieve goals and standards defined in Phase I. Throughput potential is the major difference among all candidates. Section 6, "Trade Off Studies" qualifies and quantifies throughput potential by means of the performance model.

5. TRADEOFF AND COST STUDIES - AIRBORNE

5.1 SAMPLE AND HOLD AMPLIFIERS

Both monolithic and hybrid sample and hold amplifiers (one required per data channel, in remote unit) were investigated. The hybrid S/H offers a 20 nsec aperture time at 1.88 watts and \$230 per channel; whereas the monolithic S/H has a 50-nsec aperture time for only 0.16 watts and \$35 per channel. Since even a 50-nsec aperture time results in negligible error (.06 dB at 20 KHz, from Table E-6), the choice is quite clear to proceed with the lower power monolithic S/H.

5.2 DIGITAL FILTER POWER

A study was performed to determine the effects of the system dynamic range requirements on the power required by the digital filter multiplier circuit in the control unit. (The multiplier represents an appreciable fraction of the digital filter power requirements). The results are displayed in Figure E-10 where the system dynamic range translates directly to filter stop and rejection. The multiplier power in Figure E-10 is normalized to unity at the goal level of 66-dB rejection. The conclusion reached is that even a large compromise in dynamic range requirements would result in only a small overall savings in power. (Multiplier power could be cut in half by reducing the filter rejection by a factor of 10 to 46 dB). In fact, the 66-dB requirement appears to make optimum use of a 16-bit multiplier, since 66 dB occurs at the very end of the linear portion of the curve.

5.3 NUMBER OF CHANNELS PER REMOTE UNIT

A study was performed to evaluate the benefits and penalties resulting from varying the number of data channels per remote unit. The viewpoint taken was to keep the size of the remote unit package constant in order to show an improvement in MTBF due to lower internal temperatures with fewer channels per

remote unit. The results are shown below for a 144 channel system (tape recorders not included):

	NUMBER OF CHANNELS PER R.U.		
	<u>8</u>	<u>12</u>	<u>16</u>
NO. OF BOXES TO INSTALL	19	13	10
TOTAL VOLUME	8.31 FT ³	5.69 FT ³	4.37 FT ³
TOTAL POWER	954 W.	871 W.	832 W.
MTBF	1050 HRS	-	898 HRS

Total power increases as the number of channels per remote unit decreases, because of the extra "overhead" circuitry (party-line interface) required for the additional boxes. This extra overhead also enters into the reliability calculation to offset somewhat the expected increase in MTBF due to cooler component temperatures. The table indicates that the goal of 1000 hours MTBF could be reached with 8 channels per remote unit. However, MCAIR concludes that the slight increase in MTBF is not worth the increased volume and power requirements.

5.4 VOLUME, WEIGHT AND POWER VERSUS NUMBER OF MEASURANDS

Total aircraft resources in terms of volume, weight and power requirements for the PCM encoder/formatter and tape recorder are shown in Table E-4 as a function of the number of measurands.

5.5 CALIBRATION

As indicated in Table E-6, the major error source for System 1 is the offset voltage drift with temperature.

The offset voltages can be trimmed to zero for a given temperature for

each gain setting group, but will vary with age, temperature, and gain settings. The offset voltage could be corrected by auto nulling. That is, the input is switched to ground, during a non-sample period, and a correction voltage is supplied by either a DAC or S/H circuit. This method, however, has a major problem in that switching the amplifier out of the signal path for calibration disturbs the filter input and will introduce switching transients to the filter. In addition to switching transients, the amplifier will auto range to maximum gain for offset correction and will have to reseek its nominal setting, causing additional loss of data. The above method also requires additional power consumption and board area.

The only practical approach, without data interrupts, is to calibrate each channel over-temperature for each of the higher gain settings during manufacturing test. From the data, the coefficients for a calibration curve can be computed and supplied with each unit. Correction coefficients will only have to be applied to the higher gain settings.

This method will require that a temperature sensor circuit be incorporated into each remote box. The remote box is based on the use of thermal rails to conduct the heat to the case, which will provide a uniform thermal gradient within the box. The thermal rate of change will be extremely slow which allows the central unit to multiplex the thermal data and pack the data into the PCM stream.

The ground data reduction overhead will involve storing the thermal coefficients for each channel and correction of the data.

The interchannel phase error due to component tolerances within the filters is expected to be within 5 - 10° initially. The maximum phase error between channels will occur at the cutoff frequencies. By trimming the filter parameters the phase shift can be adjusted during manufacturing test to be

equal, so that only the residual errors due to temperature drift are left.

5.6 COST CONSIDERATIONS - ENCODER/FORMATTER

Basic cost considerations for the distributed system revolve around three major elements: Non-recurring design/development costs; Recurring costs; and Sustaining costs. The following sections will address each of these costs elements which were developed by SCI Systems, Inc.

5.6.1 NON-RECURRING COSTS

For non-recurring cost estimates the distributed system hardware can be categorized as follows:

1. Remote Unit
 - A. Front-End Amplifier
 - B. Filters
 - C. Analog/Digital Conversion
 - D. Control Logic
 - E. Power Supply
 - F. Mechanical
2. Control Unit
 - A. Data Channel Interface
 - B. Digital Filter
 - C. Data Buffer Memory
 - D. Format Controller
 - E. Tape Recorder Interface
 - F. Power Supply
 - G. Mechanical
3. Test Equipment
 - A. In-Process/End-Item Test Set
 - B. EPROM Programmer

C. Quick Look Preflight Test Set

The major headings of cost can be summarized as follows:

1. Design Analysis
2. Breadboard Development and Testing
3. Test Equipment Design, Development and Testing
4. Prototype Development and Testing
5. Qualification Unit Development and Testing

From the above a work breakdown structure can be formulated to define the tasks required for the non-recurring effort. This WBS is presented in Table E-11. A summary of non-recurring costs is shown in Table E-12. While there would obviously be some variations in cost depending on which of the three approaches is taken, the overall magnitude of the non-recurring effort makes such variations minor. More important to the cost is the number of data channels that should be implemented during breadboard evaluation and the number of remote units to be built for the prototype and qualification test phases. For the purposes of establishing this cost estimate, it is assumed that two remote units will be built for the prototype unit and two will be built for the qualification testing. Three data channels will be implemented during breadboard testing.

5.6.2 RECURRING COSTS

Once the development phase has been completed, the next consideration is the cost of procuring the qualified systems for aircraft installation. Of the three system configurations studied, the system utilizing four analog filters and two centralized digital filters has been designated the baseline system. In summary, the system consists of nine remote units each providing 16 channels of data and one control unit providing the buffer storage, format programming, and the interface to the tape recorder. To establish a baseline for

recurring costs, it has been assumed that the initial procurement program will require two complete systems, one set of programming equipment, and one quick-look test set. The cost summary for this baseline is set forth in Table E-13.

In order to achieve the reliability goal, it may be necessary to configure the system for 12 or 8 channels per RU with the housing remaining approximately the same size. The cost estimates for these configurations are shown in Table E-14 for comparison.

In practicality, the likelihood of a full nine RU complement being required is small. The RU design is such that each PC board will host two complete data channels. A more likely procurement philosophy will be to determine the number of RU locations desired and the number of channels required for each location. Under these ground rules it is more appropriate to provide pricing for an RU housing (with power supply) and for individual two-channel modules. A shopping list of the system components is shown in Table E-15. This type of flexibility is inherent in the design under consideration.

As discussed earlier, the format programming requirements can be treated in several ways. The control unit has an ultra-violet erasable PROM module which can easily be removed and replaced. As one option, several modules can be procured with standard format variations, if such standards can be defined. In this case, the module with the desired characteristics can simply be installed in the CU. A second option is to program cassettes off-line with standard formats and maintain those in the field. This approach requires procurement of only one module per CU with the PROM Programmer being used to erase and load from cassette. Thirdly, the terminal of the Programmer, along with the Programmer's microcomputer and memory, will permit the generation of formats in a manual mode. The shopping list mentioned above contains the prices of both the cassette program and the pre-programmed module.

5.6.3 SUSTAINING COSTS

The topic of sustaining costs is difficult to define and depends to some extent on the method of recurring procurement discussed previously. Elements of sustaining cost are listed below:

1. Module Replacement
2. Format Generation
3. Personnel Training
4. Pre-flight Checkout
5. Pre-installation Testing

These costs relate only to the airborne PCM system and not to the data reduction and evaluation equipment. Additionally, the costs are for procured items only since the number of people involved in the various user operations can best be determined by AFWAL/FIBG.

5.6.3.1 MODULE REPLACEMENT

Based on preliminary analyses of the reliability data, spares provisioning of certain low MTBF assemblies would appear advisable. To arrive at a more firm recommendation for spares, a much more rigid analysis should be performed. For the sake of estimating, however, the data channel module, the data buffer memory module, the format memory module, and the RU mainframe are good candidates for spares. Earlier it was assumed that two complete 144-channel systems would be procured initially. Based on that assumption, Table E-16 is a preliminary recommended spares list. It is not anticipated that any of the modules will require special conditioning but the location of the data channel modules will have to be kept up with in some manner because of the unique thermal calibration coefficients that will be required in the ground data reduction.

5.6.3.2 FORMAT GENERATION

Previous discussions have dealt with pre-programmed cassettes and pre-programmed modules to control the format for data measurements. The spares recommendation in the previous paragraph included money for an additional two modules. In the event the cassettes are desired, an additional price of \$1,800 each can be assumed. Additional PROM Programmers will cost approximately \$18,000 for small quantities (1 - 5).

5.6.3.3 PERSONNEL TRAINING

Based on recent experience with Edwards Air Force Base in a three-week training program in the use of the Airborne Test Instrumentation System, the price for a similar training program will be around \$30,000. Normal training aids such as vu-graphs, charts, operation manuals, etc., will be provided.

5.6.3.4 PRE-FLIGHT CHECKOUT

The recurring price previously discussed assumed that one pre-flight checkout test set would be purchased. The Conic "d-pad'3" decomm system rack-mounted with a simple control panel will adequately serve to check selected data outputs. An additional system will cost approximately \$38,000 (AFWAL/FIBG's existing EMR 708 system can also be used for this purpose).

5.6.3.5 PRE-INSTALLATION TESTING

The intention of the Integrated Test Set referred to in the Non-recurring Cost Section is to provide both module and end-item testing during manufacture of the PCM system. The HP calculator based automatic test equipment running off the IEEE-488 bus is an ideal tester for these applications. As mentioned earlier, some of the data channels parameters can be expected to age over a period of time. Recalibration can be accomplished using the ATE procured during the nonrecurring phase, or an additional Integrated Test Set can be purchased for around \$50,000.

5.7 COST CONSIDERATIONS - TAPE RECORDER AND REPRODUCER

Price information and an equipment list for the recommended airborne tape recorder (Sangamo Sabre XII) are given in Tables E-17 and E-18. This information is current as of 8 August 1980.

One solution to the problem of obtaining a compatible reproducer for the ground system would be to negotiate a procurement from Sangamo. However, in view of AFWAL/FIBG's substantial investment in Honeywell 96 ground recorder/reproducers (including some very recently purchased machines), it appears more cost effective to modify the heads and electronics of the Model 96 to be compatible with the airborne PCM tape recorder.

6. TRADE-OFF STUDIES - GROUND EDIT, ANALYSIS AND DISPLAY SYSTEMS

The primary basis of the trade studies on possible candidates for the ground computer system is a normalized formula for performance modeling. This formula is based on actual measured speeds, known configured quantities, and written marketing specifications. Two normalized formulas describe separate performance respectively for array processors and host computers. The final performance formula or model is a composite of these two formulas.

The array processor formula is logically divided into two parts. The first part defines performance based on the configured memory size in a ratio where unity is defined as a 256 kilobyte array processor system. This memory size in ratio to 256 KB is called MI or Memory Index. Thus, MI = 2 represents a 512 KB array processor system. The second part defines performance based equally on four measured speeds of various vendors array processor "off the shelf" routines. These routines are a real 1,024 point Fast Fourier Transform, a complex 1,024 point FFT, a 1,024 by 32 point convolution, and a 1,024 point complex vector multiply. Respectively, the time for these routines are called TRFFT, TCFFT, T32PC and TCM.

The array processor performance formula is shown in Table E-22 along with a summary for performance characteristics of seven possible array processor candidates. A cost summary for each of the candidates is provided in Table E-23. It is possible for an array processor candidate to change price even with the same vendor host computer if the operating system changes. In most cases the price of any AP candidate changes for different vendor host computers due to the hardware interface. Configuration model numbers, descriptions, and individual prices are supplied in Tables E-24 through E-29.

The host computer performance formula is shown in Table E-32. It is logically divided into five parts. The first part is a Million Operations Per

Second (MOPS) benchmark measuring central processing unit execution speed, compiler efficiency and operating system performance. This benchmark has been used by MDC since 1972. It was developed by the Astronautics division (MDAC) in Houston in 1972 for the Shuttle Mission Simulator Simulation Project. MOPS is listed in Tables E-37 and E-38, respectively, for the basic and high capacity host computers.

The second part is Memory Index (MI) which has been defined in a previous paragraph. MI = 2 for a host computer would mean a 512 KB memory configuration. Array Processor Bus Interface Rate (APBIR) is the third part of the host computer performance formula. Host Bus Rate (HBR) is the effective usable megabyte per second rate at which the main bus on the CPU can perform. HBR is the fourth part of the formula. DISK is the total DISK storage configured with formatted available space in megabytes.

MOPS is a measured, accurate quantity. HBR and APBIR are based upon marketing specifications and sometimes more reliable actual measurements provided by vendors. MI and DISK are configured user changeable quantities. The values of the five factors are summarized in Table E-33 for the 12 basic candidates and are summarized in Table E-34 for the 19 high capacity candidates. A cost summary for the 12 basic and 19 high capacity candidates is presented in Tables E-35 and E-36, respectively.

Vendors change products and prices periodically. These calculations only represent information on products and prices forecasted to be stable through the April 1980 to December 1980 timeframe. Vendors also give discounts to some corporations and agencies of the United States Government. All prices presented here are full retail list.

The array processor performance formula is combined with the host computer performance formula to produce a tool to measure throughput potential. This tool

is a performance model of the ground system candidates. An example calculation is shown in Table E-17 for the current Raytheon ATP array processor performance, Raytheon 704 host computer performance, and combined system performance of the 704 and ATP. The performance of the ATP is 1.44. The performance of the Raytheon 704 is 1.25. The combined performance of the 704 and ATP system is 1.54.

Table E-21 summary table is graphically presented in Figure E-20 for array processor candidate performance versus array processor cost. Table E-20 summary table is used to generate the graph in Figure E-19, basic and high capacity host computer candidate performance versus host computer cost. Table E-20 also summarizes the combined system performance and price of all basic candidate and high capacity host computers with the recommended Floating Point Systems AP-120B. The combined system performance versus combined cost is presented graphically in Figure E-18.

From the table in Table E-22, basic array processor candidates (excluding the Data General IAP which has too small a memory) range in performance from 5.77 to 10.16 among various vendors. High capacity array processor candidates range in performance from 8.72 to 16.24 among various vendors. The main array processor vendors are CSP, Incorporated and Floating Point Systems.

Remembering that the Raytheon ATP had performance of 1.44, the basic array processor candidates are 3.97 to 7.06 times the throughput capacity. Remembering that the Raytheon 704 has performance of 1.25, the basic host computer candidates are only 1.18 to 2.8 times the throughput capacity. The high capacity host computer candidates are 3.23 to 7.67 times the throughput capacity of the Raytheon 704. Looking at Figure E-18, the basic candidate systems are 2.27 to 3.59 times the system throughput combines capacity of the 704 and ATP. The high capacity systems are 4.57 to 8.34 times the throughput capacity of the 704 and ATP.

Since the data sampling rate and the total record time is similar between

the current AFWAL/FIBG FM System and any new proposed all PCM system, any new workload is linearly related to the increase of data channels from the present 12 to the new 60-channel (as an average) test setup and from 12 to 144 as a maximum or worst case test setup (see Reference 3). Since the existing Raytheon System has a 1.54 performance, any new proposed processing facility operating in a similar four hours per working day mode would require a system with at least a $\frac{60}{12} \times 1.54$ or 7.7 performance index to handle the average test setup or $\frac{144}{12} \times 1.54$ or 18.48 performance index to handle the worst case test setup. This eliminates the basic system candidates from handling either the 60 channel average or 144-channel worst-case test setup in a similar four-hour per working day mode. The best basic system candidate could handle the average test setup if the four-hour mode was doubled to eight hours, but doubling the four-hour mode does not allow the best basic system candidate to handle the worst case.

Most but not all high capacity system candidates can handle the nominal 60-channel average setup in the four-hour mode. Note this does not mean all 60-channel work is done in half a day. It does mean a new system with five times the workload can process information in the same length of time as the old Raytheon did 1/5 the workload if the new system has a 7.7 performance index. The best high capacity system candidate with performance larger than 9.24 could handle the worst-case 144-channel test setup if the four-hour mode was doubled to eight hours. No high capacity system candidate can handle the worst-case test setup in the four-hour mode.

For safety and growth it is not recommended to change the four-hour per working day utilization factor for the average test case of 60 channels. Changing this factor for 144 channels implies that the system heavily loaded and having users needing a fast response would have to experience twice the delay

compared to the normal AFWAL/FIBG operation mode. Economics of price, however, allows bending this factor for the 144 channel mode because frequency of occurrence will be less than the 60 channel mode.

These trade studies show that the class of ground system which would be required to maintain the current AFWAL/FIBG operational workloads with input potential increasing by factors of 5 to 12 will require a system with a minimum performance index of 7.7. Basic candidate systems are thus concluded not to be acceptable. Thus, only high capacity super minicomputers and array processors will be recommended in Section 7.

7. RECOMMENDED SYSTEM CONFIGURATION

7.1 AIRBORNE SYSTEM

MCAIR recommends the System 1 PCM encoder/formatter which uses four analog filters per measurand in the remote unit, and the time-shared digital filter in the control unit. For minimizing overall volume and power, 16 channels per remote unit are recommended. The analog filters should be adjusted for matching inter-channel phase characteristics during manufacture. Use of the temperature calibration scheme outlined in Section 5.5 is not recommended except for those applications that absolutely require .5% DC accuracy. (DC accuracy without this calibration is estimated to be 0.83% in Section 3.1). Forty-eight tape outputs should be provided in the central unit so that 144 20-KHz measurands can be accommodated with a currently available recorder. For the airborne tape recorder, the only suitable off-the-shelf unit is the Sangamo Sabre XII. Purchase of the optional ground test unit and oscilloscope display unit is recommended.

7.2 GROUND SYSTEM

MCAIR recommends two different computer ground systems depending on whether AFWAL/FIBG objectives include a multi-user and/or network environment. The Floating Point Systems array processor, Model AP-12CB with 167 ns memory as configured on Figure 48 (for Digital Equipment Corporation VAX 11/780), along with the DEC VAX 11/780 as configured on Table E-45 are recommended if multi-user and/or network environment objectives are important. If these objectives are not important the Perkin Elmer 3240 as configured on Table E-46 along with the Floating Point Systems Model AP-120B array processor as configured on Table E-28 (for Perkin Elmer - Interdata) are recommended. Both the DEC VAX 11/780 and Perkin Elmer 3240 have 2 megabytes of memory and 1,024 MB of disk storage.

The PE 3240 host computer costs \$398,950 while the DEC VAX 11/780 costs \$511,750. MCAIR recommends delaying purchase of two disk drives and controllers

until forecast of growth is defined for both the DEC and PE host computers. This delay would reduce the first expenditure for the DEC VAX 11/780 from \$511,750 to only \$423,750 and would be followed with a second expenditure of approximately \$88,000 at an appropriate time. Similiarly the first expenditure for the PE 3240 would be reduced from \$398,950 to \$324,950 to be followed with a second expenditure of approximately \$74,000. The DEC VAX 11/780 is \$112,800 more than the PE 3240 host computer, but the DEC VAX 11/780 has excellent multi-user and network capabilities.

Either the DEC or PE selection will support AFWAL/FIBG future goals and objectives, such as:

- ° Desired growth potential
- ° Forecasted workload
- ° Management limits for percent facility utilization.

8. PHASE IV RECOMMENDATIONS

Phase IV work will consist of organizing and documenting the design of the selected PCM system (airborne and ground) developed during Phases I, II, and III. The final report will list the system standards and goals developed in Phase I. It will summarize the problems, approaches, and solutions identified during Phase II. It will summarize the discarded system candidates from Phase III. The final report will also contain the following:

- ° A discussion of the advantages and disadvantages of the selected PCM system with respect to AFWAL/FIBG's current FM analog system.
- ° A comprehensive block diagram of the selected system configuration, identifying new, existing, and modified components and subsystems.
- ° A cost summary identifying non-recurring and recurring costs for new and modified components and subsystems.
- ° Ground system drawings of equipment rack layout and floor space utilization.

REFERENCES

1. Appendix C, "Phase II Interim Report - Application of Pulse Code Modulation (PCM) Technology to Aircraft Dynamics Data Acquisition", 28 April 1980.
2. Appendix D, Addendum No. 1 to "Phase II Interim Report - Application of Pulse Code Modulation (PCM) Technology to Aircraft Dynamics Data Acquisition", 16 May 1980.
3. MCAIR Telecon with D. Brown, AFWAL/FIBG, 22 August 1980, "Current Raytheon Ground System Utilization".
4. MIL-E-5400T, Military Specification, "General Specification for Airborne Electronic Equipment", 16 November 1979.
5. Military Standardization Handbook - Reliability Prediction of Electronic Equipment, MIL-HDBK-217C, 9 April 1979.

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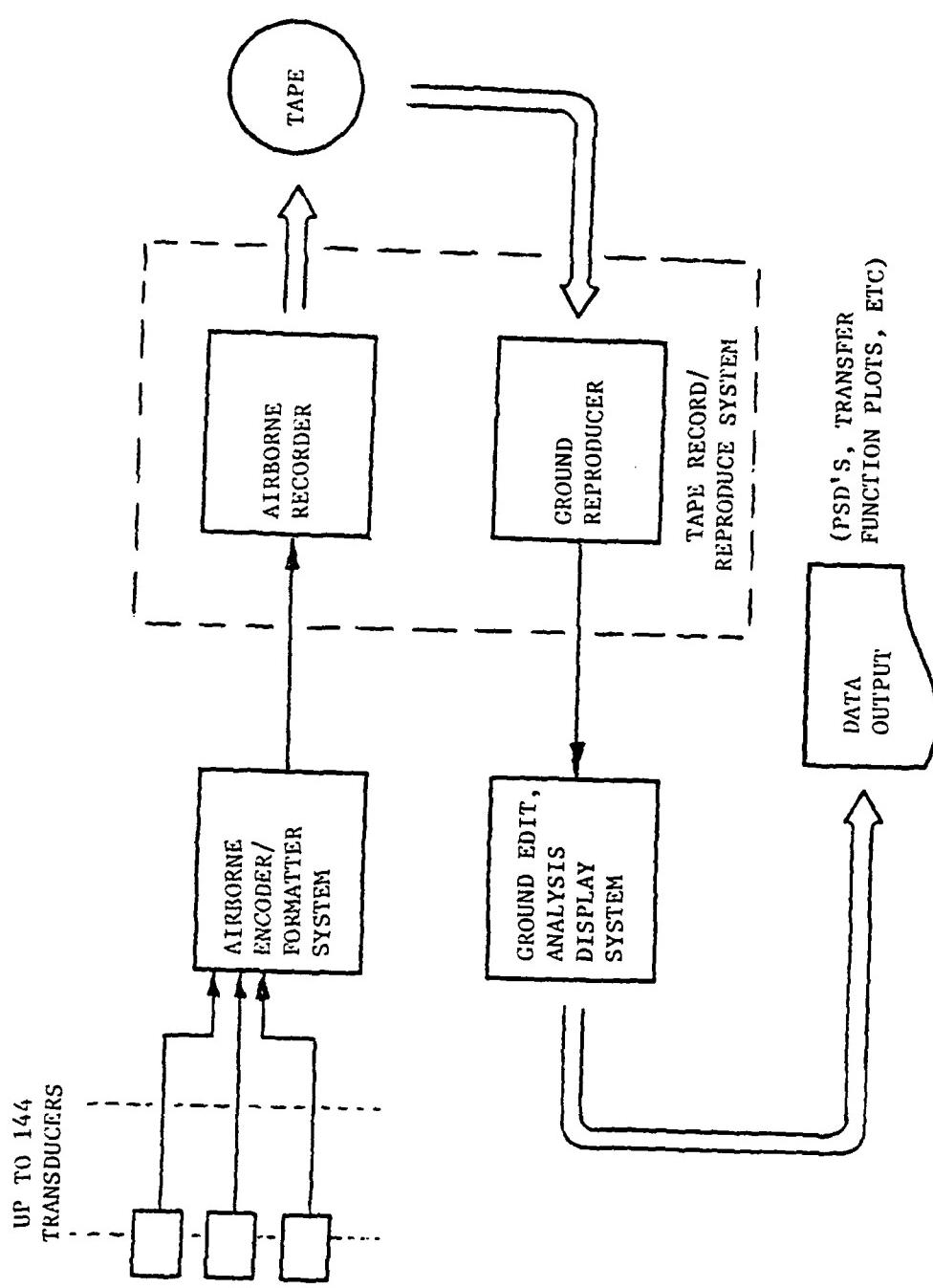


FIGURE E-1
AFMAL/FIBG PCM DATA SYSTEM

TABLE E-1
ENCODER/FORMATTER SYSTEM CHARACTERISTICS
MEETING AFWAL/FIBG GOALS

	<u>MODE A</u> <u>(TRANSIENT)</u>	<u>MODE B</u> <u>(STATIONARY)</u>	<u>MODE C</u> <u>(STATIONARY)</u>
NO. OF CHANNELS	144	144	144
FREQUENCY RANGE	DC-20KHZ	DC-20KHZ	DC-20KHZ
TIME UPDATE*	N/A	10.664 SEC	2.664 SEC
RECORD TIME	7.5 MIN	8 HRS	8 HRS
NO. OF BITS/SAMPLE	16	16	16
NO. OF FILTERS SAMPLED	1	6	5
SAMPLES PER CYCLE	3,2768	3,2768	3,2768
SAMPLE RATE COMPRESSION RATIO	1	227.5	68.2
SAMPLES PER FILTER PER UPDATE	N/A	64 TO 2048	64 TO 2048

* 512 SAMPLES PER FILTER ASSUMED FOR TIME UPDATE

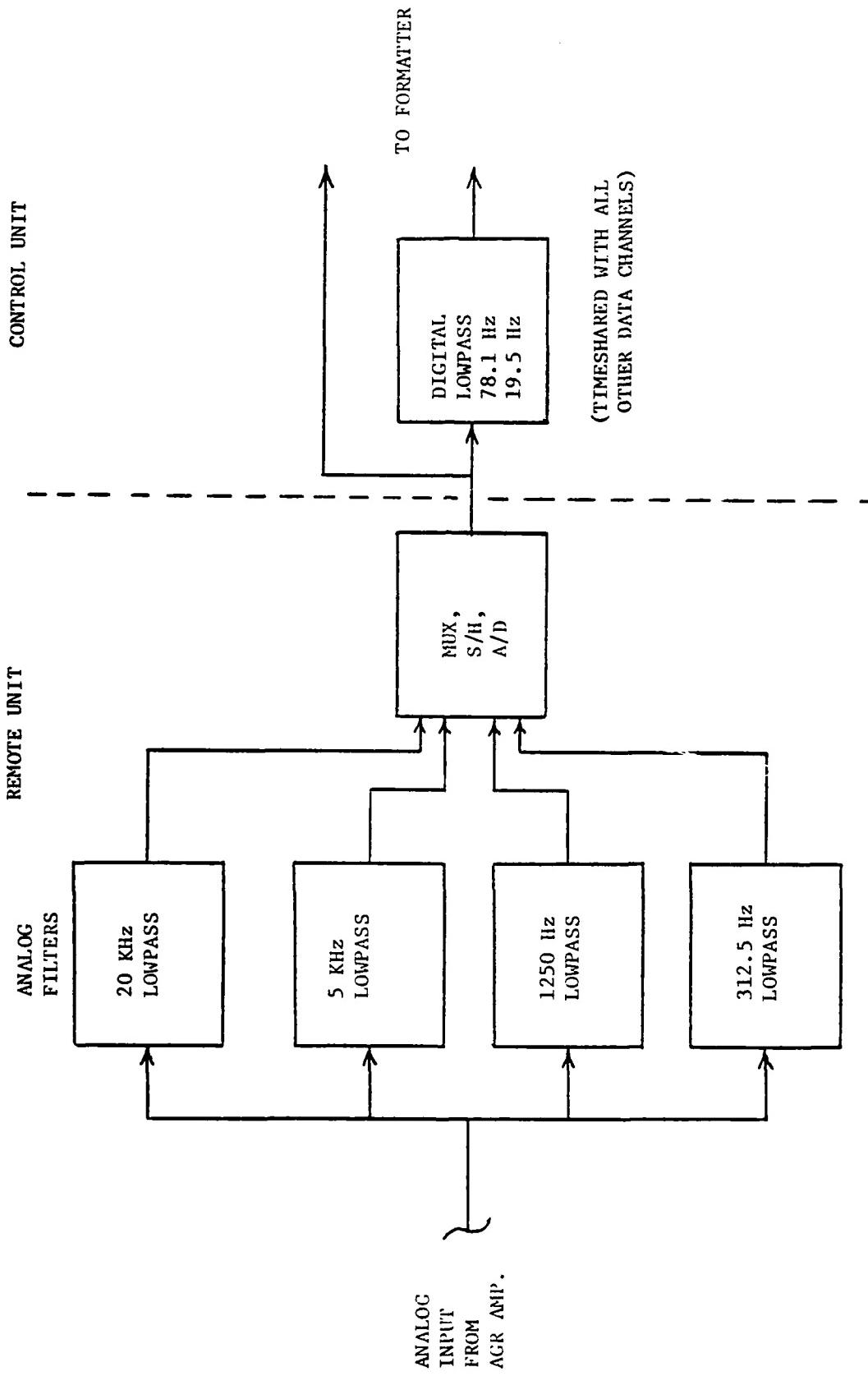


FIGURE E-2 - SYSTEM 1
FOUR VCVS ANALOG + TWO DIGITAL FILTERS

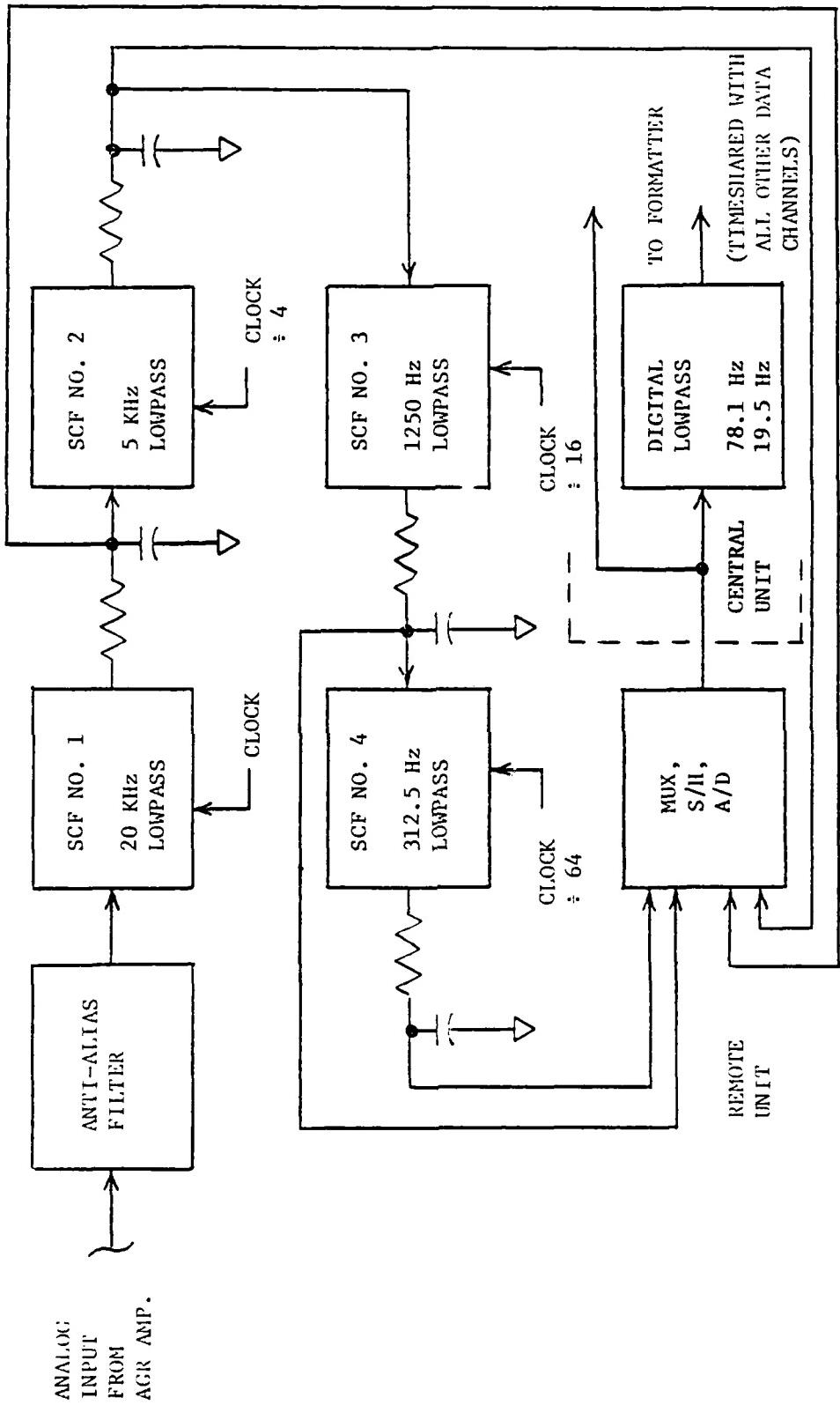


FIGURE E-3 - SYSTEM 2
FOUR SCF'S + TWO DIGITAL FILTERS

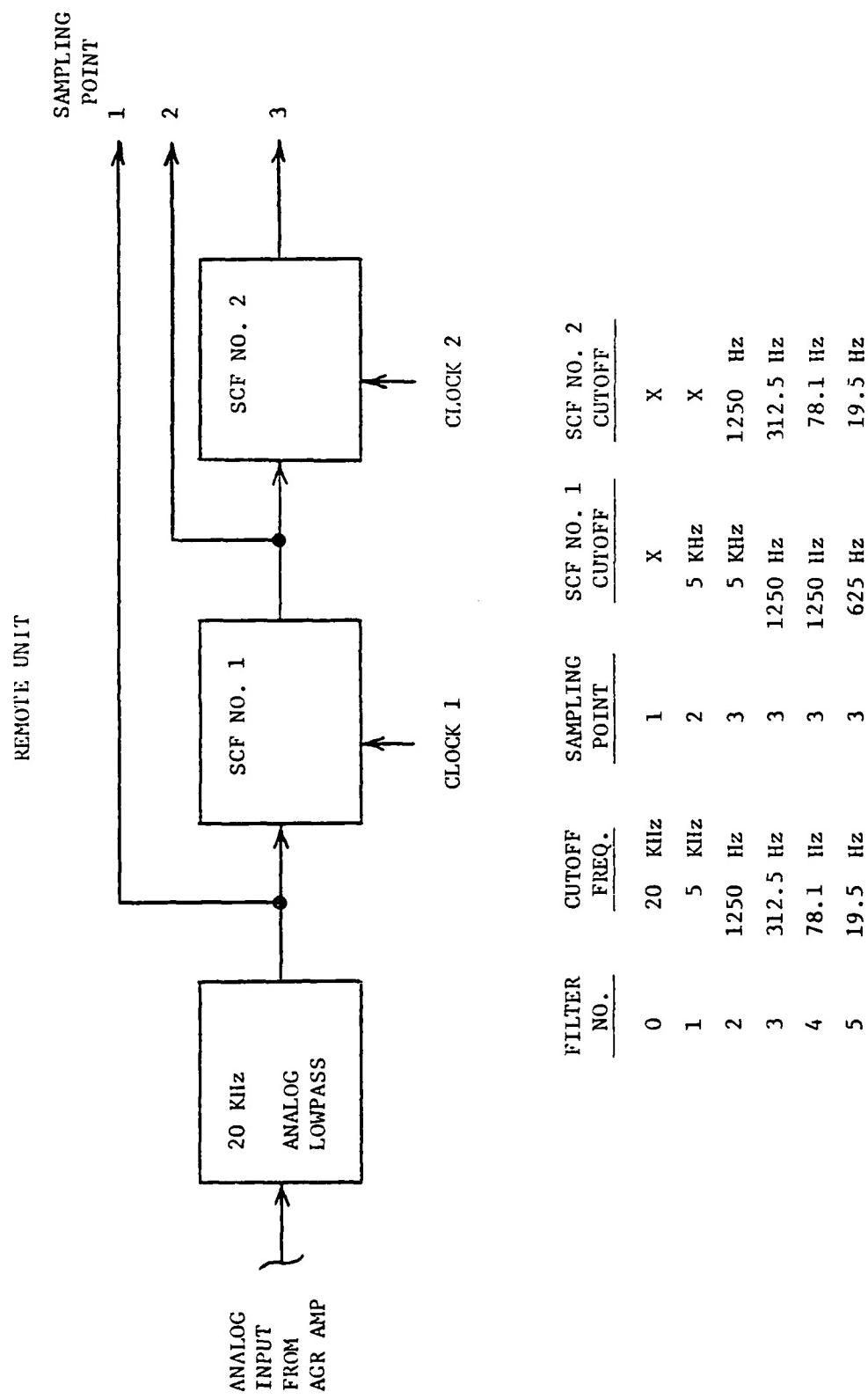


FIGURE E-4 - SYSTEM 3
ONE VCVS ANALOG + TWO VARIABLE SCF'S

TABLE E-2

ENCODER/FORMATTER OPERATING MODE	CURRENT "STATE-OF-THE-ART" CANDIDATE	FUTURE CANDIDATE
	28 TRACKS/10 1/2 INCH REEL 120 I.P.S.	28 TRACKS/14 INCH REEL 240 I.P.S.
A (7.5 MIN RECORD TIME)	48 TRACKS* 120 I.P.S. 26.8 KBPI	24 TRACKS 240 I.P.S. 26.8 KBPI
B (8 HRS RECORD TIME)	24 TRACKS 1 7/8 I.P.S. 15.1 KBPI	12 TRACKS 3 3/4 I.P.S. 15.1 KBPI
C (8 HRS RECORD TIME)	48 TRACKS* 1 7/8 I.P.S. 25.1 KBPI	24 TRACKS 3 3/4 I.P.S. 25.1 KBPI

* TWO RECORDERS REQUIRED

AIRBORNE TAPE RECORDER CHARACTERISTICS

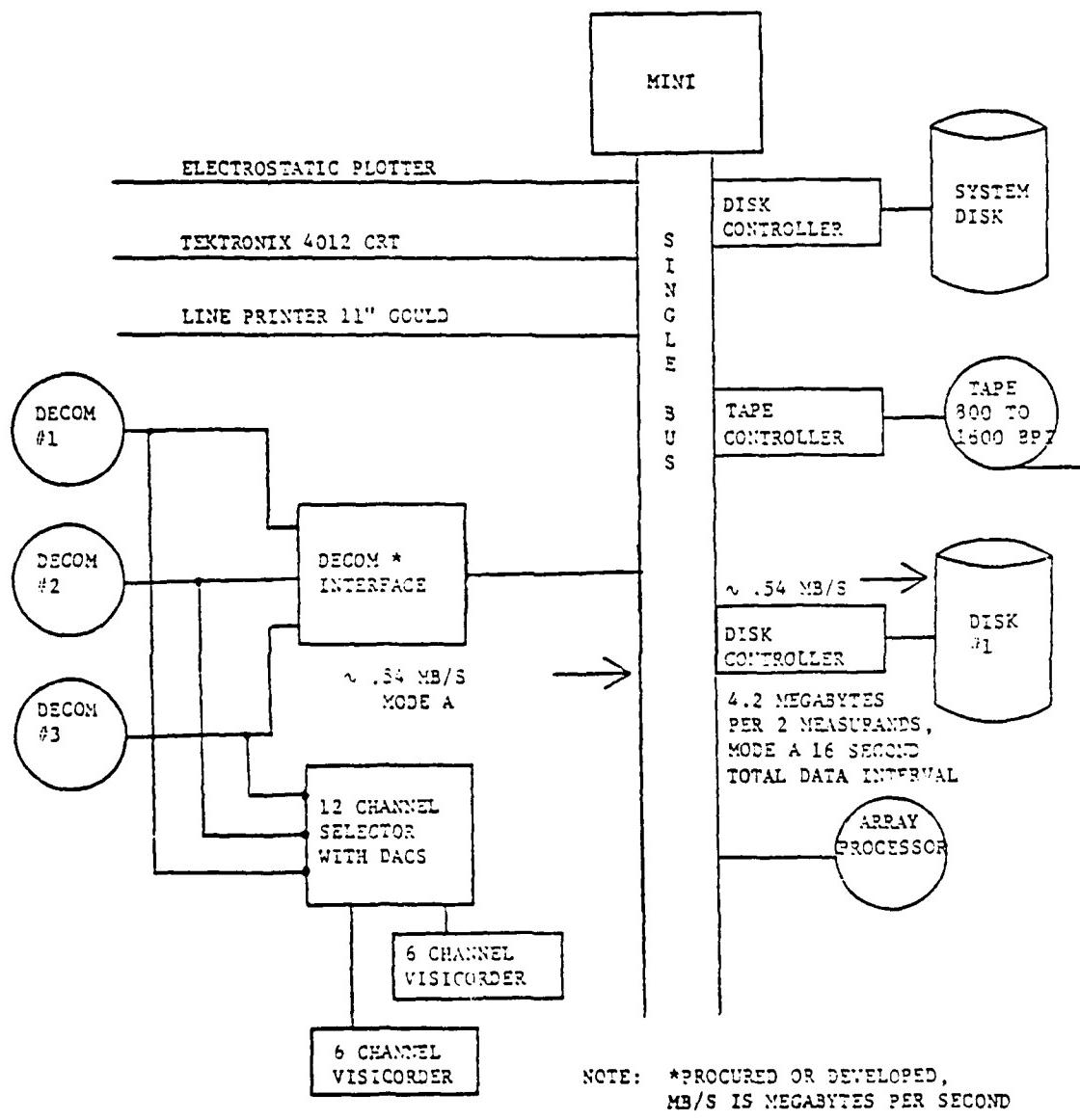
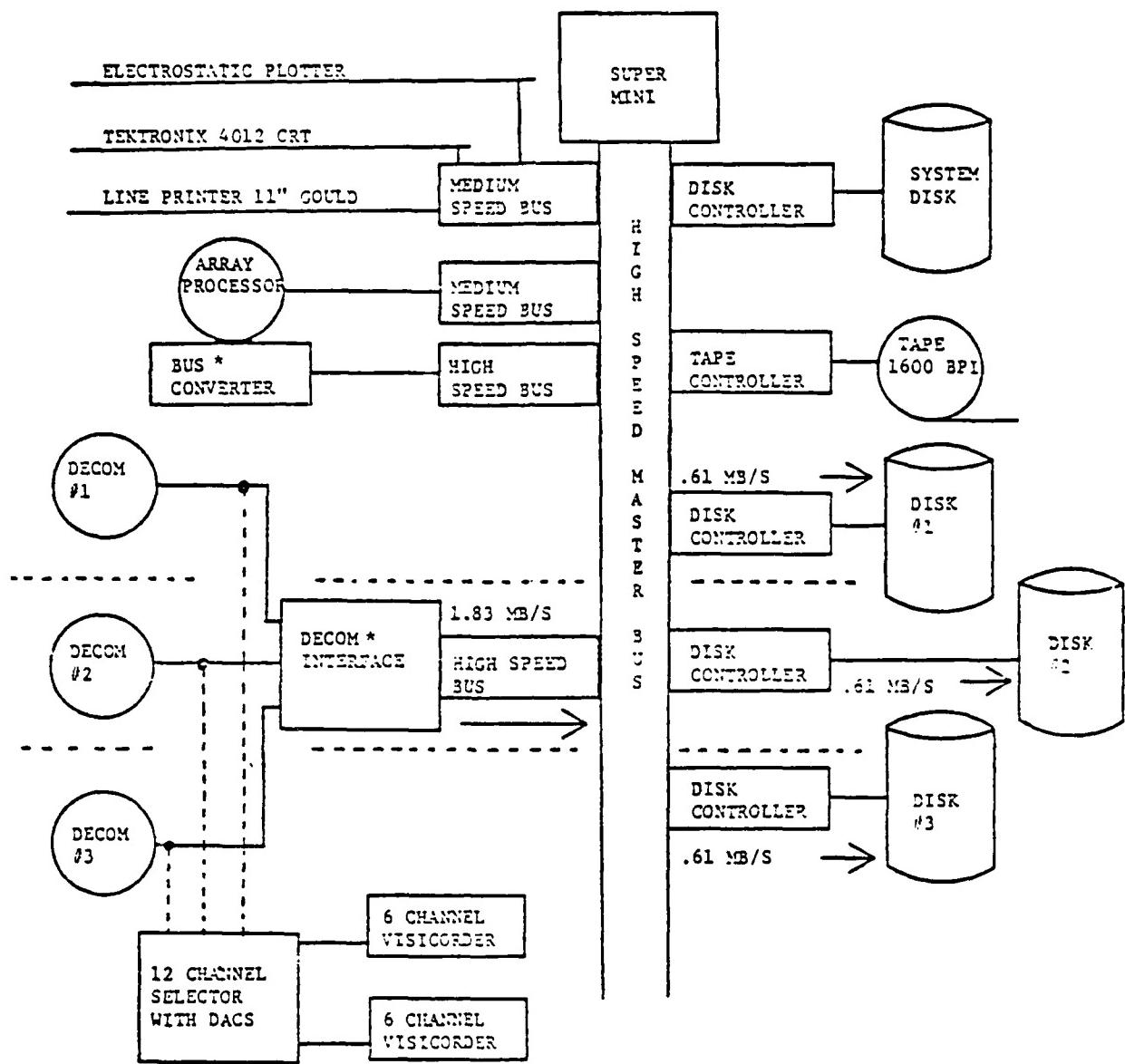


FIGURE E-5
ANALYSIS, EDIT, AND DISPLAY SYSTEM
BASIC CANDIDATE



COMMENTS:

STEP 1 - EDIT

~ 800 NEGABYTES WILL BE REQUIRED TO STORE 100% OF THE TEST TAPE ON DISK FOR 12 MEASURANDS FROM MODE A.

STEP 2 - ANALYSIS

~ 25.2 NEGABYTES TOTAL DISTRIBUTED OVER THREE DISKS ARE NEEDED TO STORE ONE SINGLE 16 SECOND DATA INTERVAL FOR 12 MEASURANDS FROM MODE A.

NOTE:

* PROCURED OR DEVELOPED HARDWARE, NOT "OFF THE SHELF"

FIGURE E-6
ANALYSIS, EDIT, AND DISPLAY SYSTEM
HIGH CAPACITY CANDIDATE

TABLE E-3
EVALUATION SUMMARY AIRBORNE ENCODER/FORMATTER AND RECORDER

CANDIDATE SYSTEMS CONFIGURATIONS
BASED ON FILTER IMPLEMENTATION

STANDARD	GOAL	SYSTEM 1		SYSTEM 2		SYSTEM 3	
		4 VCVS + 2 D	4 SCF + 2 D	4 SCF + 2 D	4 SCF + 2 D	1 VCVS + 2 VARIABLE SCF	1 VCVS + 2 VARIABLE SCF
1. BANDWIDTH/MEASURAND	DC TO 20KHZ ($\pm 10\%$)	DC TO 20KHZ ($\pm 10\%$)	DC TO 20KHZ ($\pm 10\%$)	DC TO 20KHZ ($\pm 10\%$)	DC TO 20KHZ ($\pm 10\%$)	DC TO 20KHZ ($\pm 10\%$)	DC TO 20KHZ ($\pm 10\%$)
2. ACCURACY	.5% @ DC	.5% @ DC	.5% @ DC	.5% @ DC	.5% @ DC	.5% @ DC	.5% @ DC
3. ENCODING RESOLUTION	12 BITS PLUS 3 BITS AUTO-RANGE	12 BITS PLUS 3 BITS AUTO-RANGE	12 BITS PLUS 3 BITS AUTO-RANGE	12 BITS PLUS 3 BITS AUTO-RANGE	12 BITS PLUS 3 BITS AUTO-RANGE	12 BITS PLUS 3 BITS AUTO-RANGE	12 BITS PLUS 3 BITS AUTO-RANGE
4. DYNAMIC RANGE	66 DB PLUS 70 DB AUTO-RANGE	66 DB PLUS 70 DB AUTO-RANGE	66 DB PLUS 70 DB AUTO-RANGE	66 DB PLUS 70 DB AUTO-RANGE	66 DB PLUS 70 DB AUTO-RANGE	66 DB PLUS 70 DB AUTO-RANGE	66 DB PLUS 70 DB AUTO-RANGE
5. NUMBER OF MEASURANDS	144	144	144	144	144	144	144
6. INTER-CHANNEL PHASE ERROR	5° @ 10KHZ	3°	<3°	<3°	<3°	<15°	<15°
7. RECORD TIME	A) TRANSIENT B) STATIONARY	7.5 MINUTES 8.0 HOURS	7.5 MINUTES 9.0 HOURS	7.5 MINUTES 8.0 HOURS	7.5 MINUTES 8.0 HOURS	7.5 MINUTES 8.0 HOURS	7.5 MINUTES 8.0 HOURS
8. PHYSICAL	A) SIZE B) WEIGHT C) MOBILITY	2.0 CUBIC FEET 50 POUNDS N.D.	7.8 CUBIC FEET 378 POUNDS 7.05				
9. ENVIRONMENTAL CONDITIONS	MIL E-5400, CLASS 2	MIL E-5400, CLASS 2	MIL E-5400, CLASS 2	MIL E-5400, CLASS 2	MIL E-5400, CLASS 2	MIL E-5400, CLASS 2*	MIL E-5400, CLASS 2*
10. POWER	112 WATTS @ 28 VDC	1371 W. 898 HOURS	1371 W. 898 HOURS	1371 W. 898 HOURS	1371 W. 898 HOURS	1371 W. 898 HOURS	1371 W. 898 HOURS
11. RELIABILITY	N.O.	*	*	*	*	*	*
12. MAINTAINABILITY	N.D.	*	*	*	*	*	*
13. ITSI READINESS	N.D.	*	*	*	*	*	*
14. CAPABILITY FOR ON-SITE EVAL.	ALWAYS	ALWAYS	ALWAYS	ALWAYS	ALWAYS	ALWAYS	ALWAYS
15. OPERATIONAL FLEXIBILITY	N.D.	*	*	*	*	*	*
16. RECURRING MANPOWER SUPPORT	N.D.	*	*	*	*	*	*
17. SYSTEM HARDWARE COSTS	N.D.	*	*	*	*	*	*

N.D. = GOAL NOT DECLARED

* = SEE TEXT

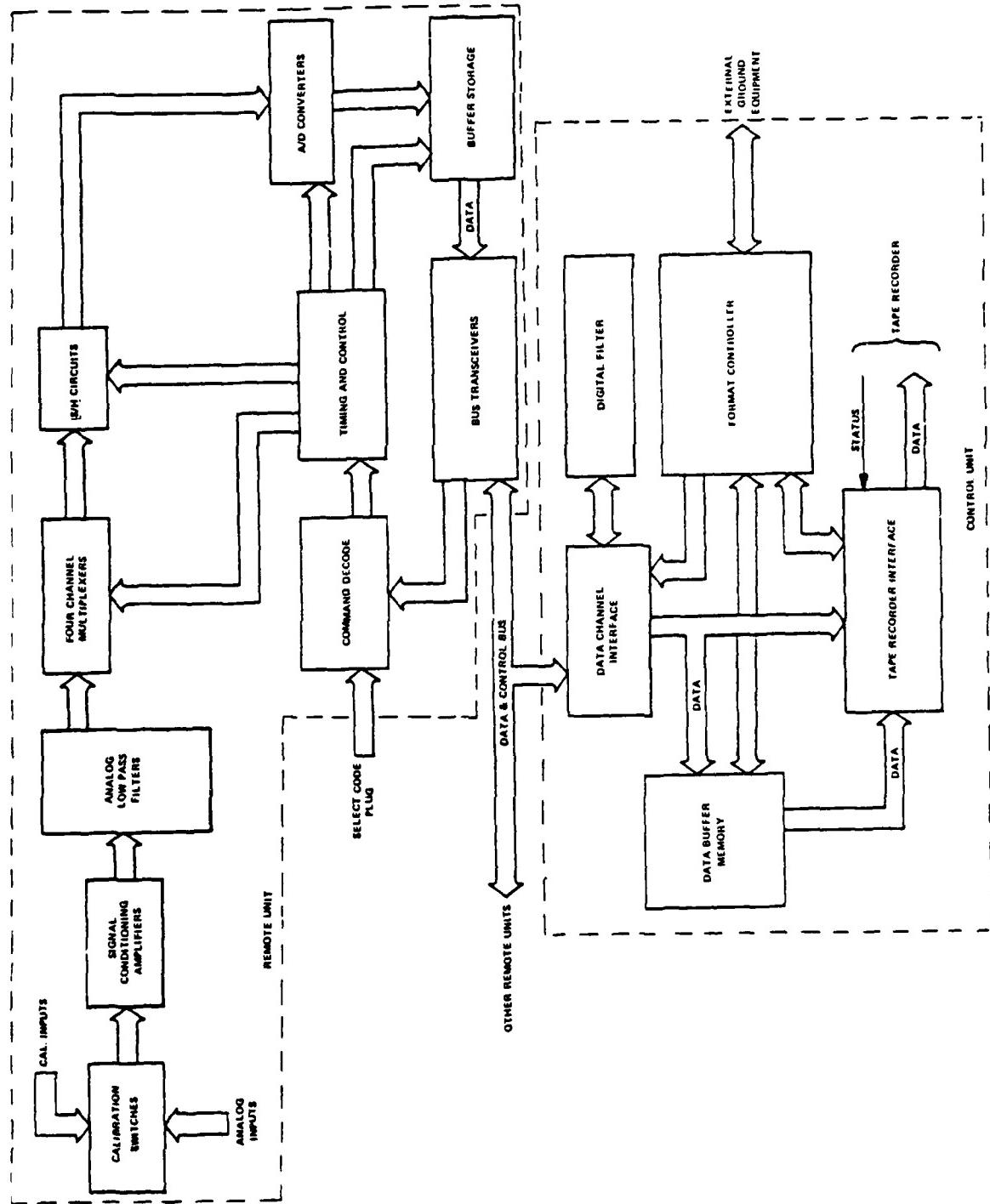
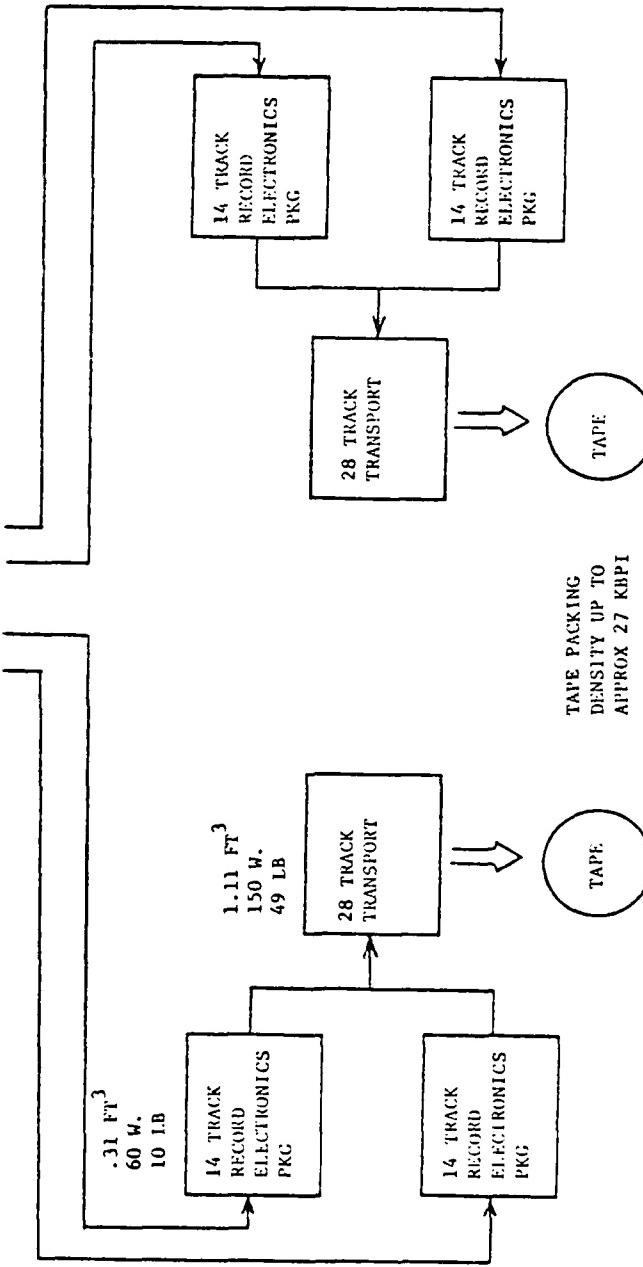


FIGURE E-7
BLOCK DIAGRAM OF DISTRIBUTED PCM SYSTEM

DATA UP TO APPROXIMATELY 154 MB/SEC FOR 7.5 MINUTES
OR UP TO APPROXIMATELY 2.3 MB/SEC FOR 8 HOURS



TWO 10 1/2 INCH REEL RECORDER REQUIRED TO MEET GOALS IF 120 I.P.S. IS MAXIMUM SPEED
A SINGLE 14 INCH REEL RECORDER COULD MEET GOALS AT 240 I.P.S.

FIGURE E-8
AIRBORNE RECORDER SYSTEM

TABLE E-4
 TOTAL AIRBORNE VOLUME, WEIGHT, POWER
 VS. NO. OF MEASURANDS
 (SYSTEM 1, 16 CH. R.U., 'STATE OF THE ART' TAPE RECORDER)

NO. OF MEASURANDS	NO. OF R.U.	NO. OF			NO. OF			TOTAL			TOTAL POWER
		TAPE	TRACKS	TRANSPORTS	RECORD	UNITS	VOLUME	WEIGHT	WEIGHT	POWER	
1 - 16	1	1 - 6		1		1	2.29 FT ³	107 LR	387W.		
17 - 32	2	6 - 11	1	1			2.73	131	469		
33 - 42	3	11 - 14	1	1			3.17	155	550		
43 - 48	3	15 - 16	1	2			3.48	165	610		
49 - 64	4	17 - 22	1	2			3.92	189	692		
65 - 80	5	22 - 27	1	2			4.35	213	774		
81 - 84	6	27 - 28	1	2			4.79	237	856		
85 - 96	6	29 - 32	2	3			6.21	296	1066		
97 - 112	7	33 - 38	2	3			6.65	320	1148		
113 - 126	8	38 - 42	2	3			7.09	344	1229		
127 - 128	8	43	2	4			7.40	354	1289		
129 - 144	9	43 - 48	2	4			7.83	378	1371		

TABLE E-5
ERROR ANALYSIS SUMMARY

Δ DC ACCURACY	FREQ. RESPONSE	INTER-CHANNEL PHASE ERROR		ALIASING ATTENUATION
		$\pm 10\text{B}$	$\pm 3^\circ \Delta$	
SYSTEM 1	$\pm .83\%$	$\pm 10\text{B}$	$\pm 3^\circ \Delta$	66dB
SYSTEM 2	$\pm 3.65\%$	$\pm 10\text{B}$	$< \pm 15^\circ$	66dB
SYSTEM 3	$\pm 2.46\%$	$\pm 0.70\text{B}$	$\pm 15^\circ$	38dB

Δ R.S.S. (OFFSET ERRORS) + R.S.S. (GAIN ERRORS)

Δ AFTER TRIMMING OF INDIVIDUAL FILTERS

TABLE E-6
ERROR ANALYSIS FOR THE THREE CANDIDATE
AIRBORNE ENCODER/FORMATTER SYSTEMS

SOURCE OF ERROR	DC ERRORS		FREQUENCY RESPONSE		ALIASING ATTENUATION
	OFFSET	GAIN	GAIN	PHASE (INTER-CH.)	
AGR AMPLIFIER	.63%	.01%	.05dB	1.7°	*
ANALOG FILTERS					
SYSTEM 1	.02%	*	1dB	2.4°	66dB
SYSTEM 2	1.4%	2.1%	1dB	<15°	66dB
SYSTEM 3	0.7%	1.5%	.7dB	<15°	38dB
MULTIPLEXER	*	.01%	*	*	*
SAMPLE AND HOLD	.01%	*	.06dB	.18°	*
A/D CONVERTER	.09%	.19%	*	*	*

* = NOT APPLICABLE OR VIRTUALLY NO ERROR

Δ = DC TO 20KHz

Δ = MEASURED AT 10KHz

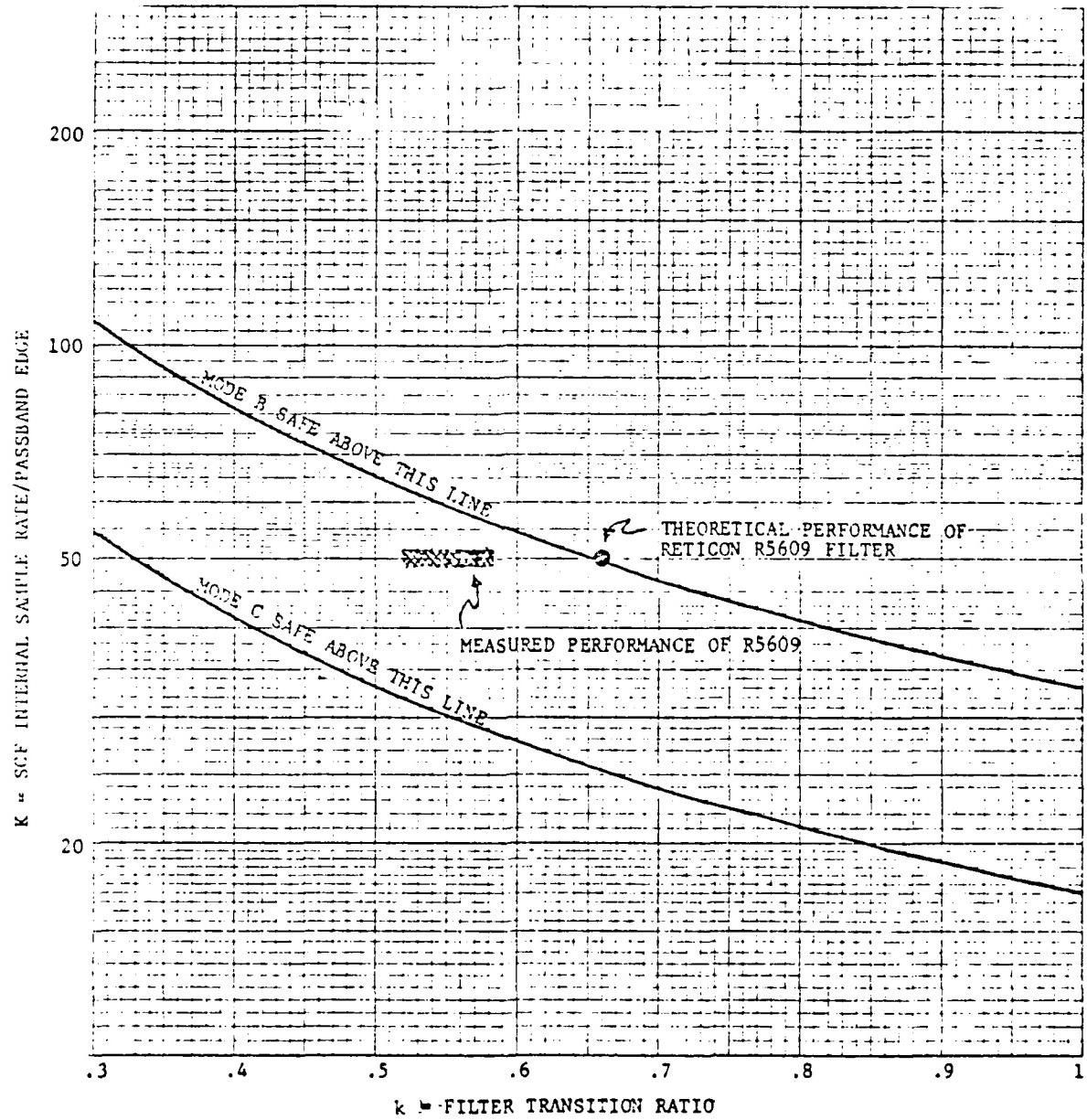


FIGURE E-9
 SYSTEM 3 ONE VCVS + TWO SCF
 EVALUATION OF ANTI-ALIASING PROTECTION

TABLE E-7
CONTROL UNIT POWER DISSIPATION

SYSTEM FILTER IMPLEMENTATION

	NO. 1 <u>4 VCYS + 2D</u>	NO. 2 <u>4 SCF + 2D</u>	NO. 3 <u>1 VCYS + 2SCF</u>
PARTY LINE INTERFACE	9.5 W.	9.5 W.	9.5 W.
DIGITAL FILTERS	21	21	0
DATA BUFFER MEMORY	4	4	4
TAPE RECORDER INTERFACE (24 - 48 TAPE TRACKS)	8 - 16	8 - 16	8 - 16
FORMATTER	16	16	16
SUB TOTALS	58.5 - 66.5 W.	58.5 - 66.5 W.	37.5 - 45.5 W.
LOSS IN 70% EFFICIENT POWER SUPPLY	25.1 - 28.5 W.	25.1 - 28.5 W.	16.1 - 19.5 W.
TOTAL POWER DISSIPATED IN CONTROL UNIT	83.6 - 95.0 W.	83.6 - 95.0 W.	53.6 - 65.0 W.

TABLE E-8
16 CHANNEL REMOTE UNIT POWER DISSIPATION

	SYSTEM FILTER IMPLEMENTATION		
	NO. 1 <u>4 VCVS + 2D</u>	NO. 2 <u>4 SCF + 2D</u>	NO. 3 <u>1 VCVS + 2 SCF</u>
SIGNAL CONDITIONERS	13.2W.	13.2W.	13.2W.
ANALOG FILTERS	12.8	14.1	10.2
A/D CONVERTERS	19.2	19.2	19.2
SAMPLE AND HOLD	2.6	2.6	2.6
PARTY LINE INTERFACE	<u>9.5</u>	<u>9.5</u>	<u>9.5</u>
SUB-TOTALS	57.3W.	58.6W.	54.7W.
LOSS IN 70% EFFICIENT POWER SUPPLY	24.6W.	25.1W.	23.4W.
TOTAL REMOTE UNIT POWER	81.9W.	83.7W.	78.1W.

TABLE E-9
 REMOTE UNIT (SYSTEM 1, 4 VCVS + 2D)
 POWER DISSIPATION VERSUS NO. OF CHANNELS

	<u>8 CH. PER</u> <u>R.U.</u>	<u>12 CH. PER</u> <u>R.U.</u>	<u>16 CH. PER</u> <u>R.U.</u>
SIGNAL CONDITIONERS	6.6W.	9.9W.	13.2W
ANALOG FILTERS	6.4	9.6	12.8
A/D CONVERTERS	9.6	14.4	19.2
SAMPLE AND HOLD	1.3	1.9	2.6
PARTY LINE INTERFACE	<u>9.5</u>	<u>9.5</u>	<u>9.5</u>
SUB-TOTALS	33.4W.	45.3W.	57.3W.
LOSS IN 70% EFFICIENT POWER SUPPLY	14.3W.	19.4W.	24.6W.
TOTAL REMOTE UNIT POWER	47.7W.	64.7W.	81.9W.

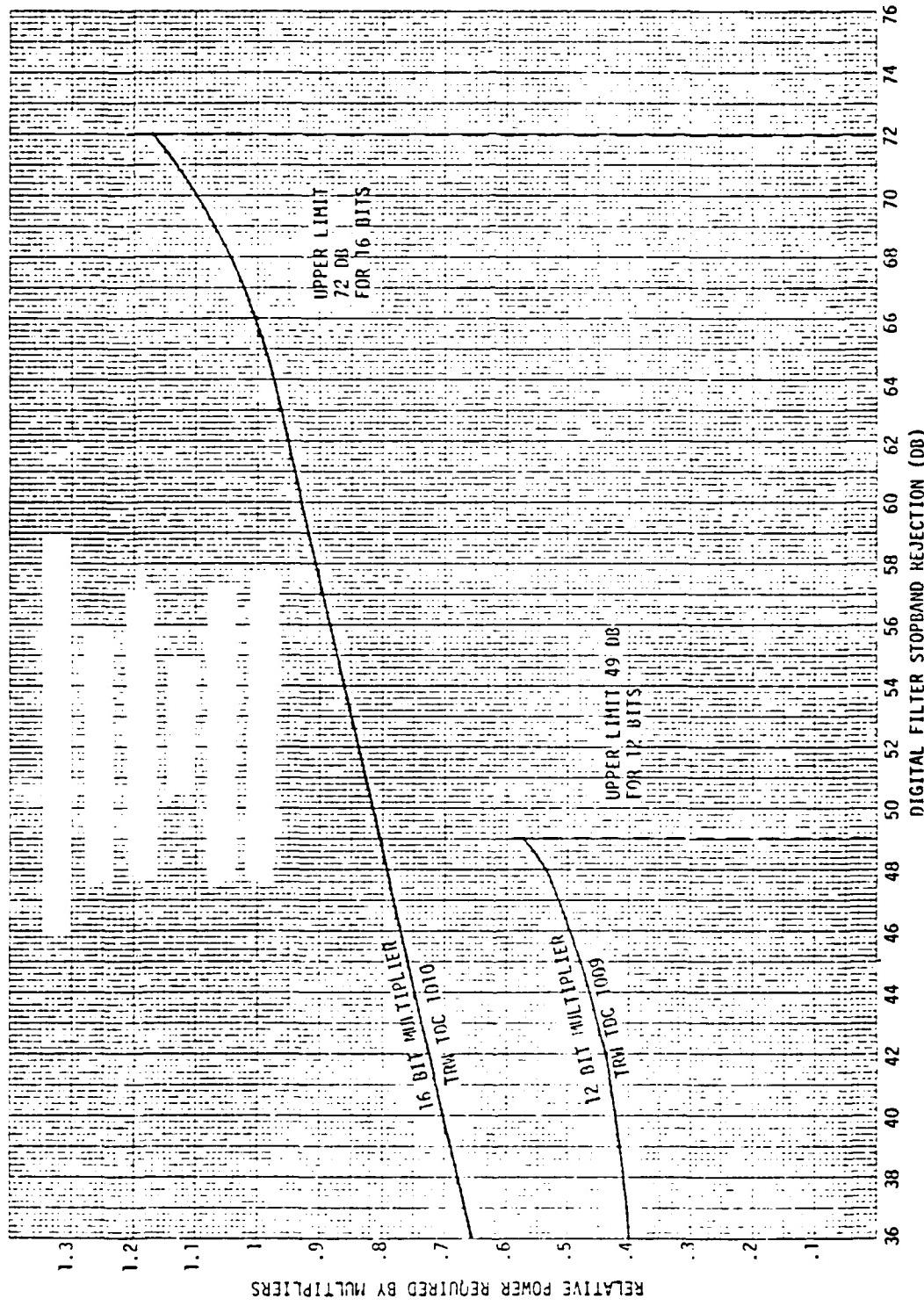


FIGURE E-10
MULTIPLE FILTER CONFIGURATION 3A, FIR DIGITAL FILTERS
RELATIVE MULTIPLIER POWER VS. FILTER STOPBAND REJECTION PASSBAND ERROR .2 dB (P-P)

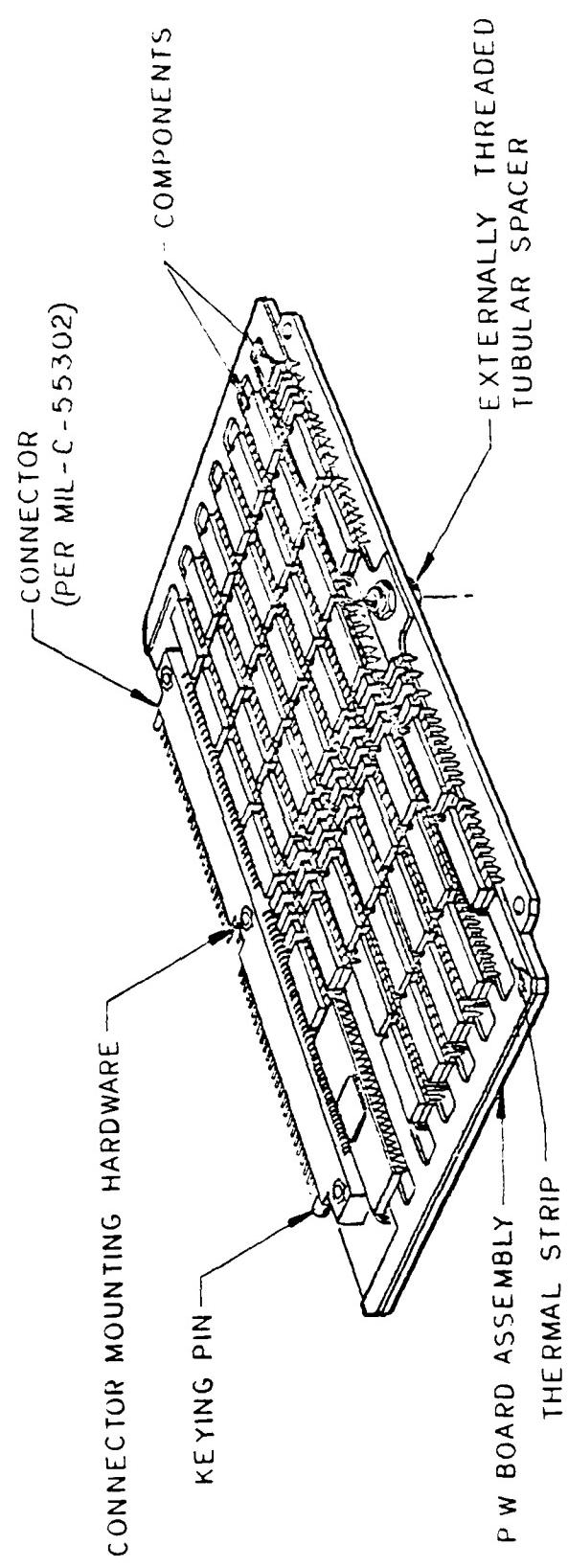


FIGURE E-11
TYPICAL PC BOARD CONSTRUCTION

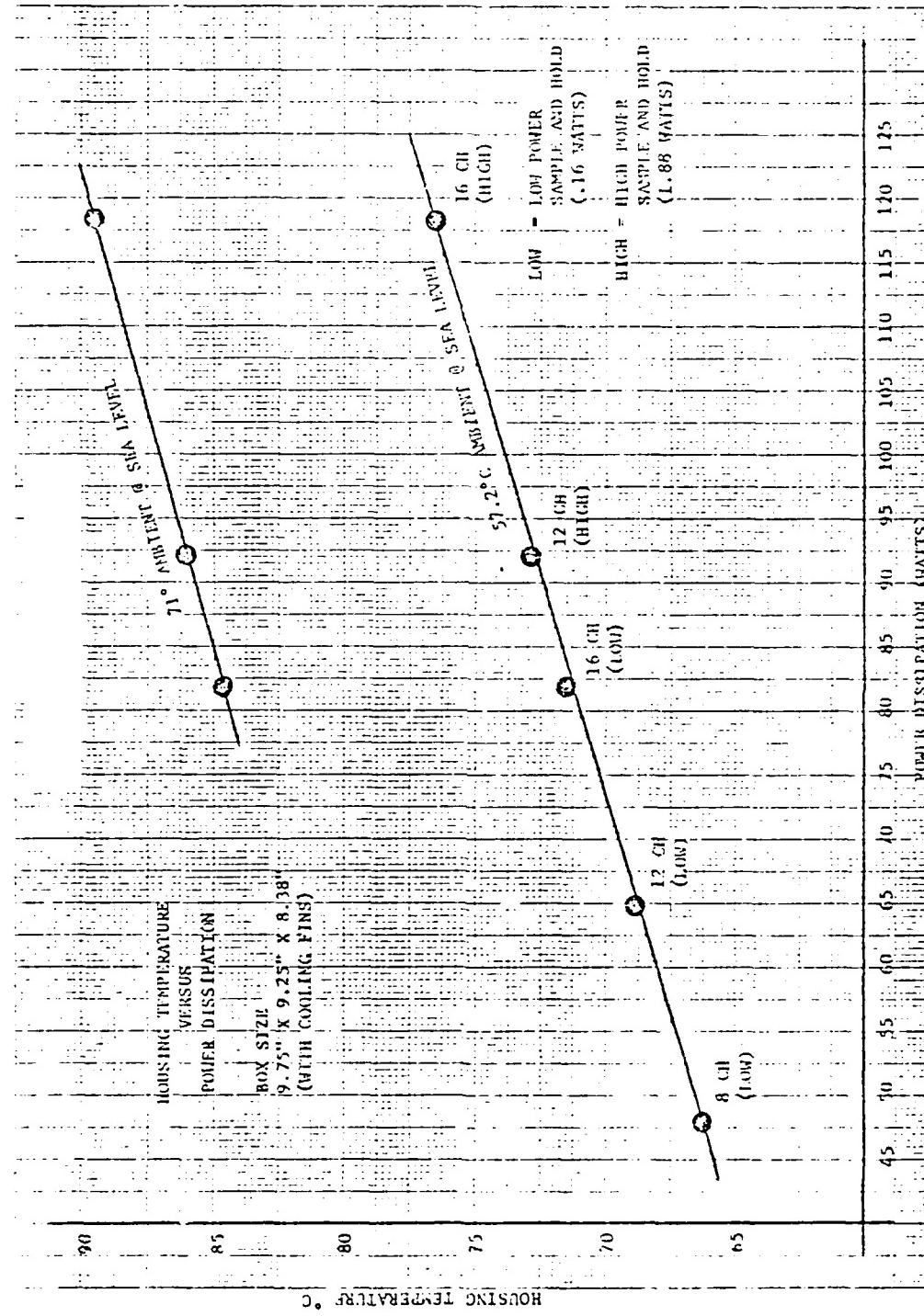


FIGURE E-12
 THERMAL ANALYSIS SUMMARY
 REMOTE UNIT

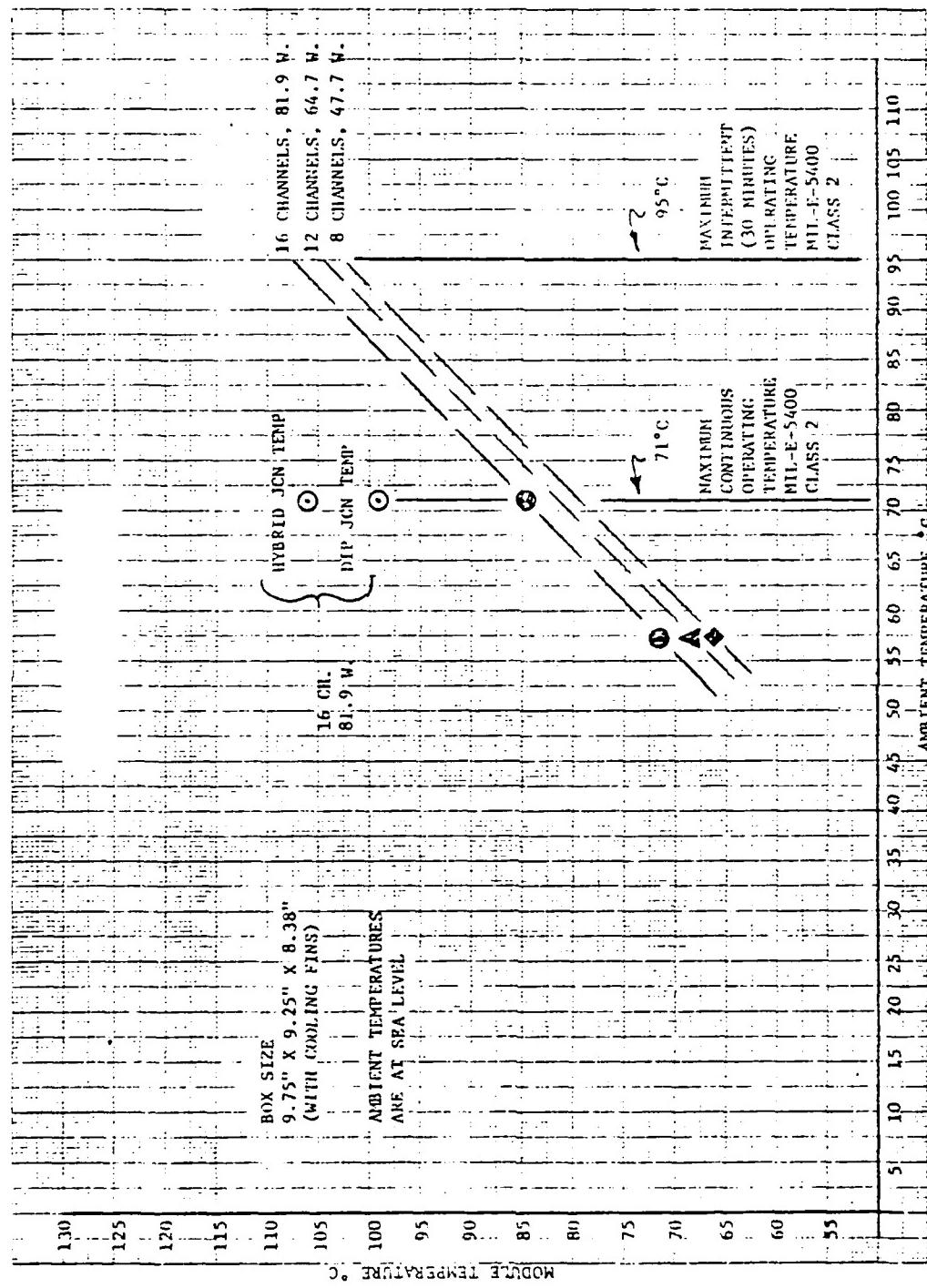


FIGURE E-13
THERMAL ANALYSIS SUMMARY
REMOTE UNIT

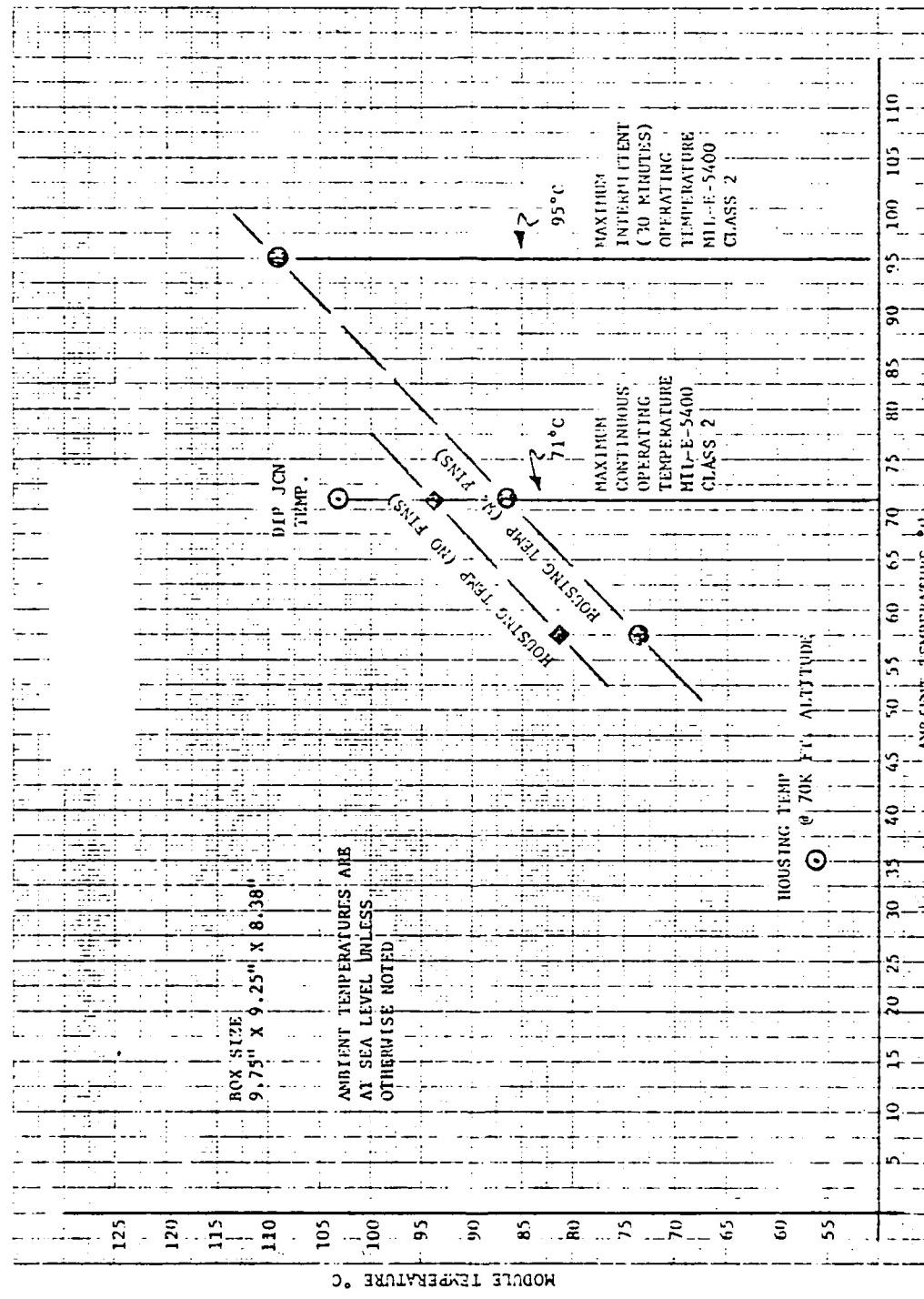


FIGURE E-14
THERMAL ANALYSIS SUMMARY
CENTRAL UNIT
(95 WATTS)

TABLE E-10
AIRBORNE ENCODER/FORMATTER
RELIABILITY ESTIMATE

	<u>FAILURE RATE</u> <u>% PER 1000 H</u>
<u>16 CHANNEL REMOTE UNIT</u>	
AGR AMPLIFIERS	3.43
ANALOG FILTERS	
SYSTEM 1	2.63
SYSTEM 2	3.48
SYSTEM 3	2.40
MULTIPLEXER	0.64
SAMPLE AND HOLD	0.30
A/D CONVERTER	0.25
PARTY-LINE INTERFACE	0.85
POWER SUPPLY	<u>2.55</u>
REMOTE UNIT TOTALS SYSTEM 1	10.65
SYSTEM 2	11.50
SYSTEM 3	10.42
<u>CONTROL UNIT</u>	
CONTROL (INCLUDES PARTY-LINE INTERFACE)	10.30
DIGITAL FILTER (NOT USED IN SYSTEM 3)	2.63
POWER SUPPLY	<u>2.55</u>
CONTROL UNIT TOTALS SYSTEMS 1 AND 2	15.48
SYSTEM 3	12.85
144 CHANNEL SYSTEM RELIABILITY (9 REMOTE UNITS + 1 CONTROL UNIT)	
SYSTEM 1:	111.33%/1000 HOURS, 898 HOURS MTBF
SYSTEM 2:	118.98%/1000 HOURS, 840 HOURS MTBF
SYSTEM 3:	106.63%/1000 HOURS, 938 HOURS MTBF

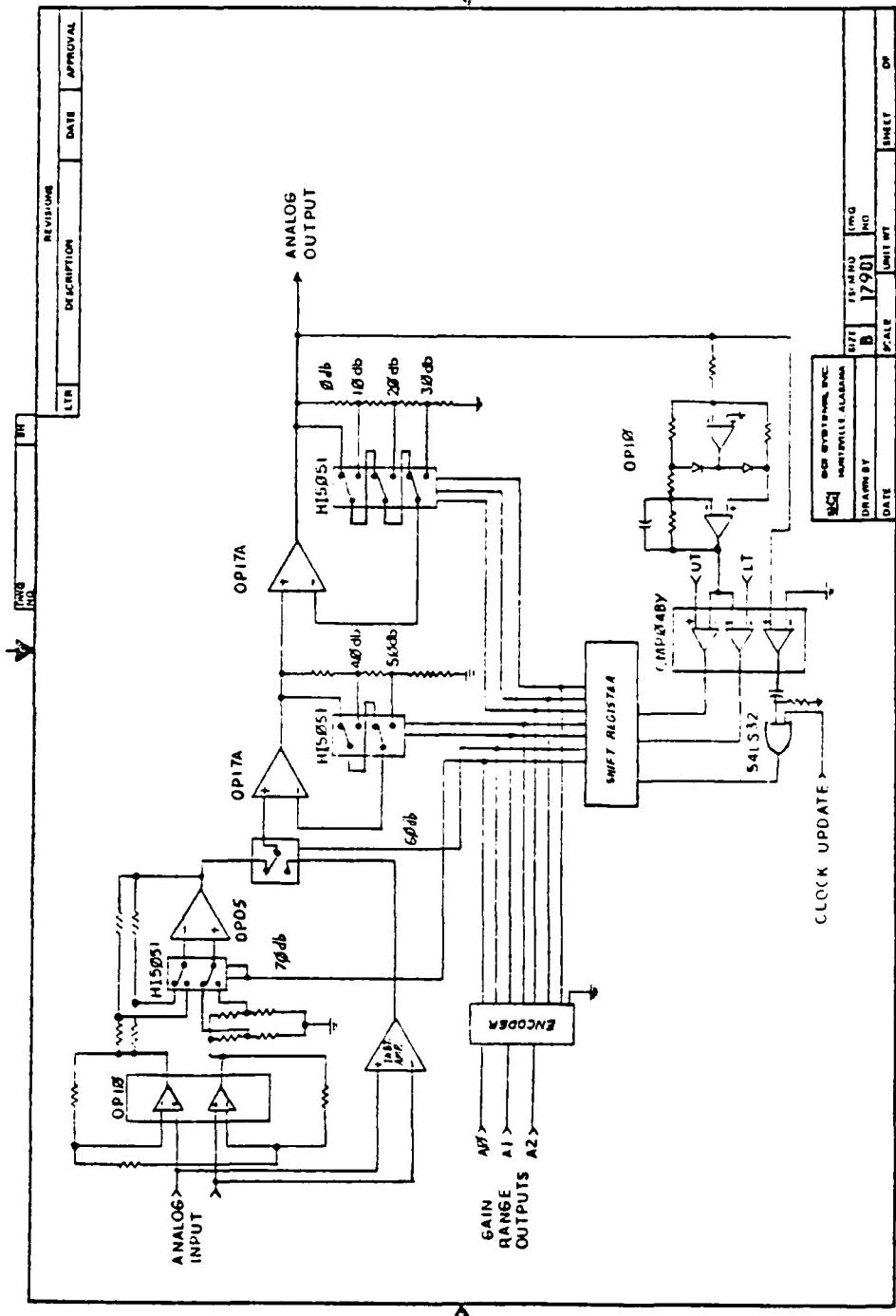


FIGURE E-15
AGR AMPLIFIER

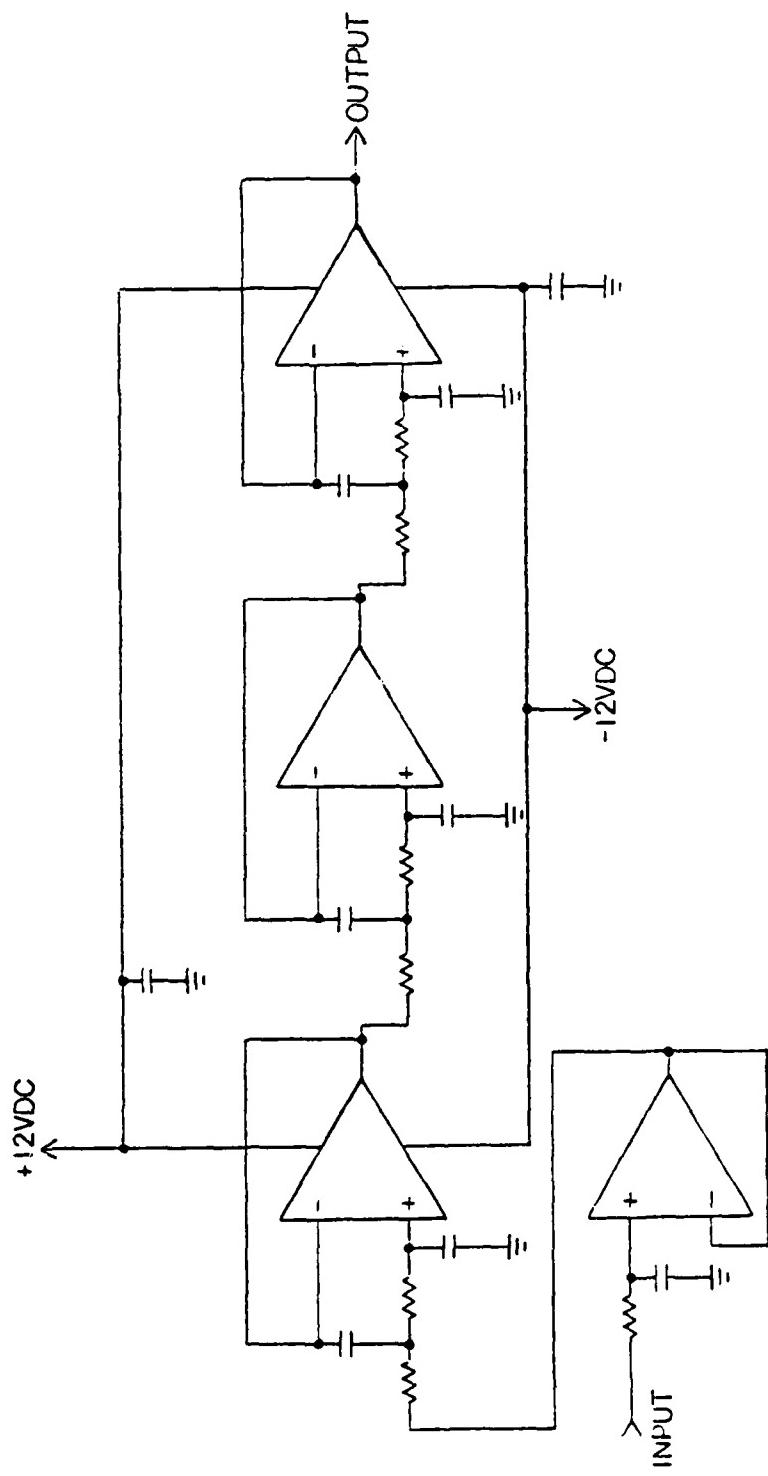


FIGURE E-16
7-POLE CHEBYSHEV LOWPASS VCVS FILTER

TABLE E-11
WORK BREAKDOWN STRUCTURE
NON-RECURRING

1.0 DESIGN, DEVELOPMENT, TEST AND EVALUATION

1.1 DESIGN ANALYSES

1.1.1 Remote Unit

1.1.1.1 Front End Amplifiers
1.1.1.2 Filters
1.1.1.3 ADC
1.1.1.4 Control Logic
1.1.1.5 Power Supply
1.1.1.6 Mechanical Design

1.1.2 Control Unit

1.1.2.1 Data Channel Interface
1.1.2.2 Digital Filter
1.1.2.3 Data Buffer Memory
1.1.2.4 Format Controller
1.1.2.5 Tape Recorder Interface
1.1.2.6 Power Supply
1.1.2.7 Mechanical Design

1.1.3 Development Data

1.1.3.1 Development Test Plan
1.1.3.2 Software Development Plan
1.1.3.3 Prelim System Specification
1.1.3.4 Thermal Analysis
1.1.3.5 Reliability Analysis

1.1.4 Concept Design Review

1.2 BREADBOARD DEVELOPMENT

1.2.1 Remote Unit

1.2.1.1 Front-end Amplifiers
1.2.1.2 Filters
1.2.1.3 ADC

1.2.1.4 Control Logic
1.2.1.5 Power Supply

1.2.2 Control Unit

1.2.2.1 Data Channel Interface
1.2.2.2 Digital Filter
1.2.2.3 Data Buffer Memory
1.2.2.4 Format Controller
1.2.2.5 Tape Recorder Interface
1.2.2.6 Power Supply

1.2.3 Data

1.2.3.1 Schematics
1.2.3.2 Parts Program Plan
1.2.3.3 Outline Drawings
1.2.3.4 Weight Analysis

1.2.4 Preliminary Design Review

1.3 PROTOTYPE DEVELOPMENT AND TESTING

1.3.1 Remote Unit (2 Ea)

1.3.1.1 System Engineering
1.3.1.2 Fabrication
1.3.1.3 Test

1.3.2 Control Unit (1 Ea)

1.3.2.1 System Engineering
1.3.2.2 Fabrication
1.3.2.3 Test

1.3.3 System Integration & Test

1.3.4 Documentation

1.3.4.1 Production Documentation
1.3.4.2 Acceptance Test Procedure
1.3.4.3 Development Test Report
1.3.4.4 System/Subsystem Specifications
1.3.4.5 Programming Manual

1.3.5 Critical Design Review

1.4 QUALIFICATION UNIT DEVELOPMENT & TEST

1.4.1 Remote Unit (2 Ea)

- 1.4.1.1 System Engineering
- 1.4.1.2 Fabrication
- 1.4.1.3 Test

1.4.2 Control Unit

- 1.4.2.1 System Engineering
- 1.4.2.2 Fabrication
- 1.4.2.3 Test

1.4.3 System Integration and Test

1.4.4 Data & Documentation

- 1.4.4.1 Qualification Test Procedure
- 1.4.4.2 Qualification Test Report
- 1.4.4.3 Documentation Clean-up

1.4.5 Final Design Review

1.5 TEST EQUIPMENT

1.5.1 Integrated Test Set

- 1.5.1.1 Design & Software Development
- 1.5.1.2 Fabrication/Procurement (1 Ea)
- 1.5.1.3 Verification Testing

1.5.2 EPROM Programmer

- 1.5.2.1 Design & Software Development
- 1.5.2.2 Fabrication/Procurement (1 Ea)
- 1.5.2.3 Verification Testing

1.5.3 Quick-Look Pre-Flight Test Set

- 1.5.3.1 Design & Software Development
- 1.5.3.2 Fabrication/Procurement (1 Ea)
- 1.5.3.3 Verification Testing

TABLE E-12
NON-RECURRING COST SUMMARY (\$ THOUSANDS)

NON-RECURRING
COST SUMMARY (\$ THOUSANDS)

1.1	DESIGN ANALYSIS	135.0
1.1.1	Remote Unit	45.0
1.1.2	Control Unit	65.0
1.1.3	Development Data	15.0
1.1.4	Concept Design Review	10.0
1.2	BREADBOARD DEVELOPMENT	123.0
1.2.1	Remote Unit	45.0
1.2.2	Control Unit	60.0
1.2.3	Data	8.0
1.2.4	Preliminary Design Review	10.0
1.3	PROTOTYPE DEVELOPMENT	204.0
1.3.1	Remote Unit Fab & Assy (2 ea)	60.0
1.3.2	Control Unit Fab & Assy	34.0
1.3.3	Test	60.0
1.3.4	Documentation/Data	40.0
1.3.5	Critical Design Review	10.0
1.4	QUALIFICATION PROGRAM	204.0
1.4.1	Remote Unit Fab & Assy (2 ea)	60.0
1.4.2	Control Unit Fab & Assy	34.0
1.4.3	Test	85.0
1.4.4	Documentation/Data	15.0
1.4.5	Final Design Review	10.0
1.5	TEST EQUIPMENT	155.0
1.5.1	Integrated Test Set	100.0
1.5.2	PROM Programmer	25.0
1.5.3	Quick-Look Test Set	30.0
1.6	SYSTEM ENGINEERING & MANAGEMENT	80.0
1.0	TOTAL DDT&E	\$901.0

TABLE E-13
SYSTEM RECURRING COST SUMMARY

<u>ITEM</u>	<u>QTY</u>	<u>\$/EA</u>	<u>\$ TOTAL</u>
Control Unit	2	30,000	60,000
Remote Unit	18	26,100	469,800
PROM Programmer	1	21,000	21,000
Quick-Look Test Set	1	38,000	38,000
			<hr/>
			\$588,800

TABLE E-14
RECURRING COSTS
CONFIGURATION OPTIONS

	12 Channel RU			8 Channel RU		
	<u>Qty</u>	<u>Unit Price</u>	<u>Total</u>	<u>Qty</u>	<u>Unit Price</u>	<u>Total</u>
Control Unit	2	\$30,000	\$60,000	2	\$30,000	\$60,000
Remote Unit	24	21,000	504,000	36	15,000	540,000
PROM Programmer	1	21,000	21,000	1	21,000	21,000
Quick-Look Test Set	1	38,000	38,000	1	38,000	38,000
			<u>\$623,000</u>			<u>\$659,000</u>

TABLE E-15
PCM SYSTEM
SHOPPING LIST

Remote Unit

Data Channel Module	\$3,000*
Interface Assembly	2,000
Power Supply	2,500
Mainframe	1,000

Control Unit

Interface Module	3,000
Tape Recorder Module	6,000
Data Buffer Memory	8,500
Format Controller	3,500
Format Memory Module	3,200
Digital Filter Module	3,000
Power Supply	2,500
Mainframe	1,000

Integrated Test Set

50,000

Quick-Look Test Set

38,000

PROM Programmer

21,000

Programmed Cassette

1,800

* AVERAGE PRICE FOR QUANTITY OF 25 TO 50.

TABLE E-16
PRELIMINARY RECOMMENDED SPARES LIST

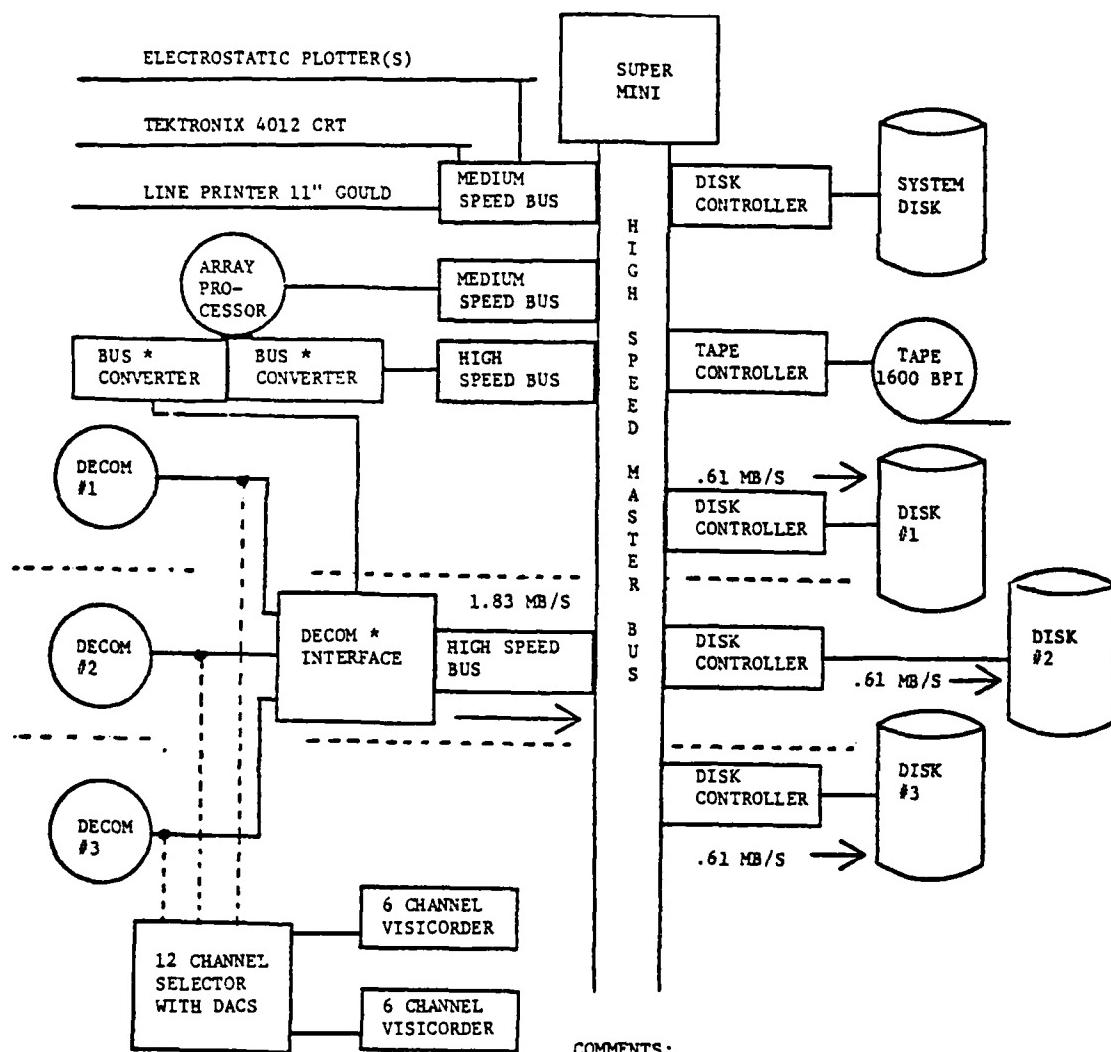
<u>ITEM</u>	<u>BASIC ORDER Q'TY</u>	<u>SPARES Q'TY</u>	<u>\$/EA</u>	<u>\$/TOTAL</u>
RU Mainframe	18	1	1,000	1,000
RU Power Supply	18	1	2,500	2,500
Data Channel Module	144	5	3,000	15,000
RU Control Logic	18	0	-	-
CU Data Channel Interface	2	0	-	-
CU Data Buffer Memory	2	1	8,500	8,500
CU Format Controller	2	1	3,500	3,500
CU Format Memory Module	2	2	3,200	6,400
Digital Filter Module	2	1	3,000	3,000
CU Tape Recorder Interface	2	0	-	-
CU Power Supply	2	0	-	-
CU Mainframe	2	0	-	-
				39,900

TABLE E-17
AIRBORNE RECORDER - PRICE INFORMATION

QUANTITY	DESCRIPTION	UNIT PRICE	TOTAL
5	Sangamo Sabre XII airborne/severe environment magnetic tape recorder as detailed by the equipment list and Sangamo data sheet, dated April 1979.	\$53,985	\$269,925
Sabre XII Options			
1	Flight control unit (MA 7135/0)	\$ 1,110	\$ 1,110
1	Miniaturized flight control unit (MA 7135/1)	\$ 1,175	\$ 1,175
1	Ground control unit (MA 8040/0)	\$ 2,250	\$ 2,250
1	Oscilloscope display unit (MA 8031/0) (To be utilized in the ground control unit)	\$ 1,990	\$ 1,990
1	Direct reproduce amplifier (MA 2229/0)	\$ 310	\$ 310
Direct Equalizers			
1	400Hz to 2,000kHz @ 120 ips (MA 5227/7)	\$ 70	\$ 70
1	400Hz to 1,000kHz @ 60 ips (MA 5227/6)	\$ 70	\$ 70
1	400Hz to 500kHz @ 30 ips (MA 5227/5)	\$ 70	\$ 70
1	400Hz to 250kHz @ 15 ips (MA 5227/4)	\$ 70	\$ 70
1	FM reproduce demodulator (MA 1234/0)	\$ 375	\$ 375
FM Filters			
1	DC to 400 kHz (MA 5228/9)	\$ 65	\$ 65
1	DC to 200 kHz (MA 5228/8)	\$ 65	\$ 65
1	DC to 100 kHz (MA 5228/7)	\$ 65	\$ 65
1	DC to 50 kHz (MA 5228/6)	\$ 65	\$ 65
1	DC to 25 kHz (MA 5228/5)	\$ 65	\$ 65
1	DC to 12.5 kHz (MA 5228/5)	\$ 65	\$ 65
1	DC to 6.25 kHz (MA 5228/3)	\$ 65	\$ 65
1	DC to 3.125kHz (MA 5228/2)	\$ 65	\$ 65

TABLE E-18
 EQUIPMENT LIST FOR ONE (1)
 SABRE XII MAGNETIC TAPE RECORDER SYSTEM

<u>ORDER NO.</u>	<u>QTY</u>	<u>DESCRIPTION</u>
4110/11	1	1" WIDEBAND SABRE XII TRANSPORT
MA 0173/0	1	1" IRIG 28 TRACK WIDEBAND RECORD HEADS
MA 0280/0	1	1" 14 TRACK REPRODUCE HEADS TO BE UTILIZED FOR 28 TRACK REPRODUCE MONITORING
MA 8039/0	2	RACK FOR THE RECORD AMPLIFIERS (ONE REQUIRED FOR EACH FOURTEEN CHANNELS OF RECORD ELECTRONICS)
MA 8041/0	2	MOUNTING TRAY FOR MA 8039/0
MA 7148/1	1	Y CONNECTING CABLE BETWEEN THE RECORD AMPLIFIER RACKS FOR A TWENTY-EIGHT CHANNEL SYSTEM AND THE TRANSPORT (10 FEET IN LENGTH)
MA 2131/0	2	DIRECT RECORD AMPLIFIERS
MA 1143/0	2	FM RECORD MODULATORS
MA 1144/0	26	SERIAL HIGH DENSITY PCM ENCODERS
MA 7136/0	1	LOCAL COMMAND CARD (ONE OF THESE IS REQUIRED UNLESS ONE OF THE REMOTE CONTROL UNITS IS PURCHASED)
MA 7134/0	1	AIRCRAFT ANTIVIBRATION MOUNTING (3 AXIS)



COMMENTS:

STEP 1 - EDIT

~ 800 MEGABYTES WILL BE REQUIRED TO STORE 100% OF THE TEST TAPE ON DISK FOR 12 MEASURANDS FROM MODE A.

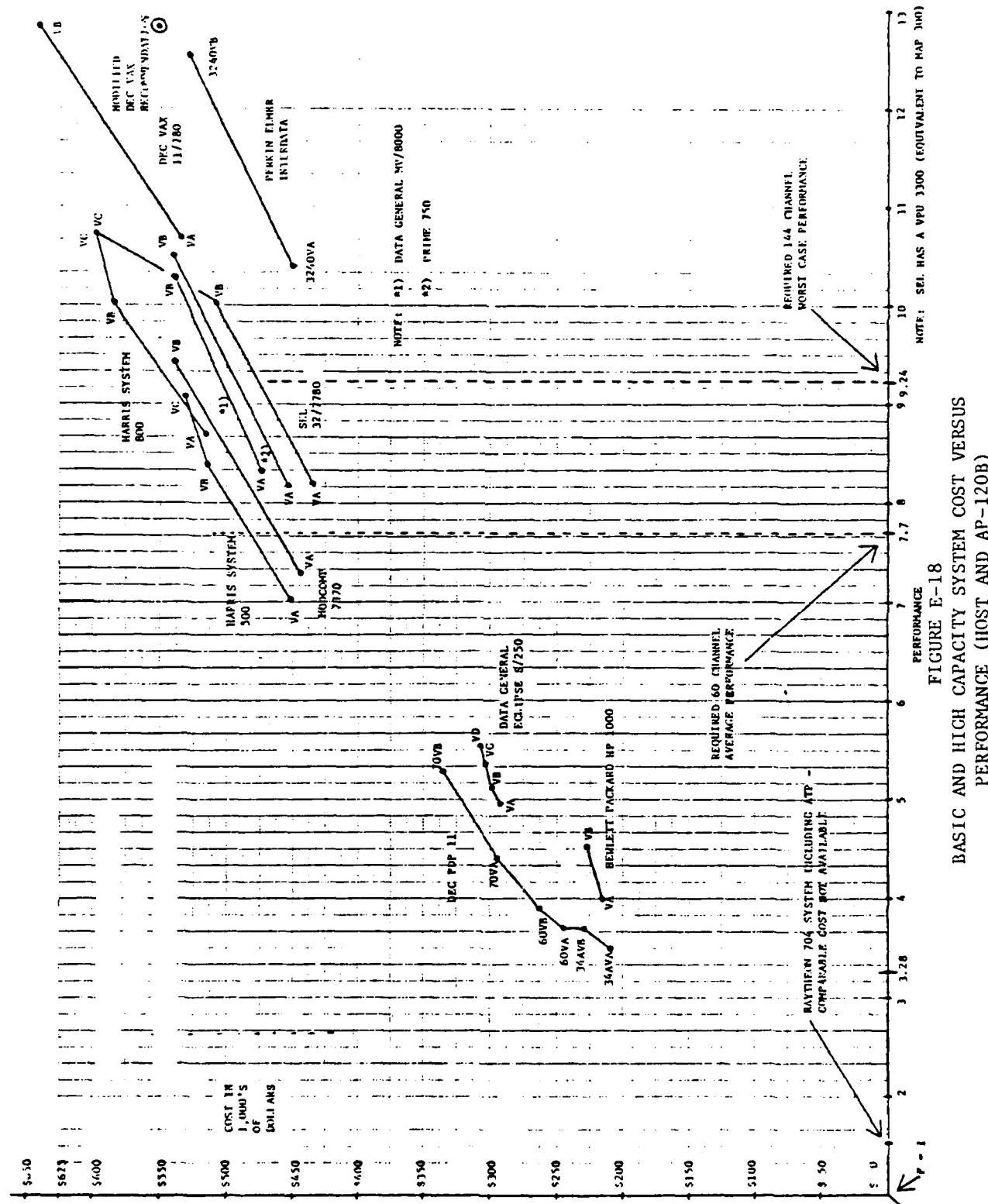
STEP 2 - ANALYSIS

~ 25.2 MEGABYTES TOTAL DISTRIBUTED OVER THREE DISKS ARE NEEDED TO STORE ONE SINGLE 16 SECOND DATA INTERVAL FOR 12 MEASURANDS FROM MODE A.

NOTE:

* PROCURED OR DEVELOPED HARDWARE, NOT "OFF THE SHELF"

FIGURE E-17
ANALYSIS, EDIT, AND DISPLAY SYSTEM
HIGH CAPACITY CANDIDATE OPTIONAL EDIT CONFIGURATION



BASIC AND HIGH CAPACITY SYSTEM COST VERSUS PERFORMANCE (HOST AND AP-120B)

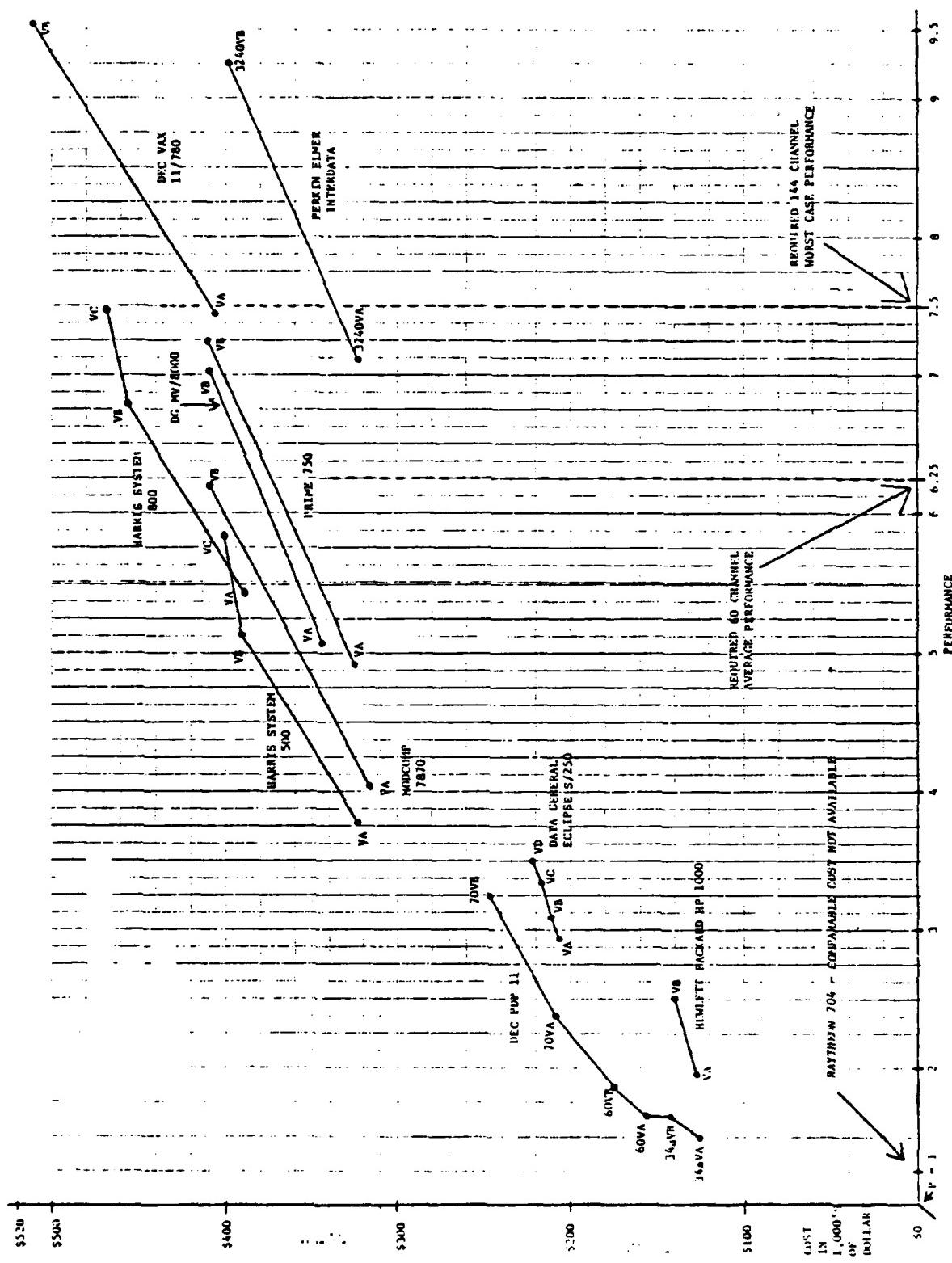


FIGURE E-19
BASIC AND HIGH CAPACITY HOST COST VERSUS PERFORMANCE

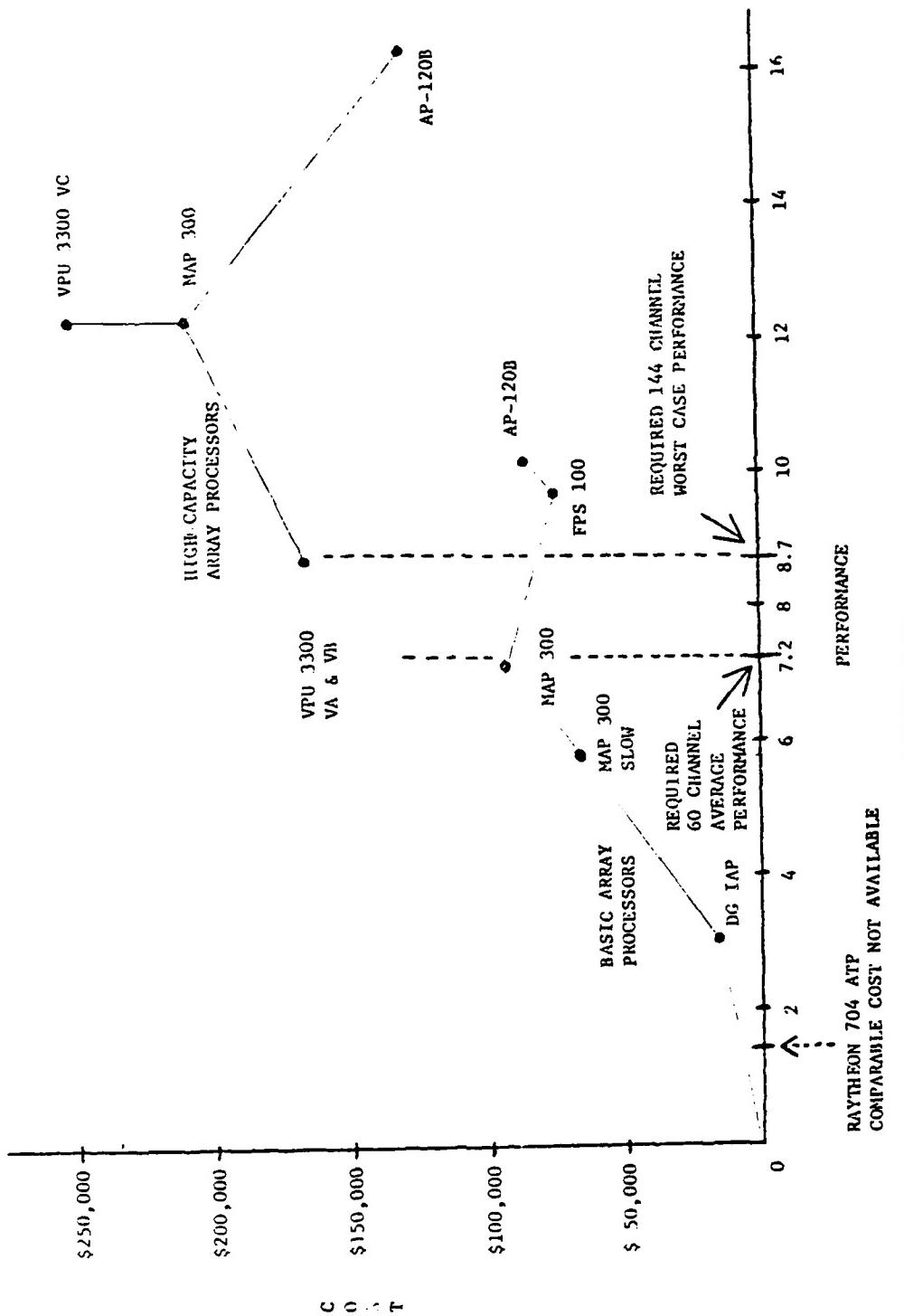


FIGURE E-20
ARRAY PROCESSOR COST VERSUS PERFORMANCE

TABLE E-19
EXISTING RAYTHEON 704 SYSTEM PERFORMANCE SUMMARY

704 ATP

MI (MEMORY INDEX) = .25
TRFFT (TIME FOR REAL 1,024 POINT FFT) = 40.8 MS
TCFFT (TIME FOR COMPLEX 1,024 POINT FFT) = 66.3 MS
T32PC (TIME FOR 1,024 BY 32 POINT CONVOLUTION) = 126 MS
TCM (TIME FOR COMPLEX VECTOR MULTIPLY) = 8.5 MS

$$\text{PERFORMANCE}_{704 \text{ ATP}} = \frac{4 \times .25}{1.133} + \frac{4.35}{40.8} + \frac{7.69}{66.3} + \frac{20.28}{126} + \frac{1.50}{8.5} = 1.443$$

704 HOST

MOPS (MILLION OPERATIONS PER SECOND) = .0294
MI = .25
APBIR (ARRAY PROCESSOR BUS INTERFACE RATE) = 2.0 MB/S
HBR (HOST BUS RATE) = 2.0 MB/S
DISK (TOTAL DISK STORAGE) = 5 MB

$$\text{PERFORMANCE}_{704 \text{ HOST}} = \frac{.0294}{.209} + \frac{.25}{4.79} + \frac{2}{2.31} + \frac{2}{11.07} + \frac{5}{575.6} = 1.248$$

704 SYSTEM

$$\text{PERFORMANCE}_{704 \text{ SYSTEM}} = 1.248 + \frac{1.443}{5} = 1.54$$

TABLE E-20
BASIC AND HIGH CAPACITY HOST AND AP SYSTEM COST,
PERFORMANCE, P/C SUMMARY

MODEL #	AP & HOST COST	P(HOST)	P/C (HOST)	P(HOST) + [P(AP)/5]	$\frac{P(HOST \& AP) \times 1,000,000}{AP \& HOST COST}$
DEC PDP 11/34A VA	\$211,925	1.47	11.73	3.5	16.52
DEC PDP 11/34A VB	230,225	1.66	11.56	3.69	16.03
DEC PDP 11/60 VA	245,175	1.66	10.47	3.69	15.05
DEC PDP 11/60 VB	263,475	1.85	10.46	3.88	14.73
DEC PDP 11/70 VA	295,275	2.38	11.41	4.41	14.94
DEC PDP 11/70 VB	334,175	3.26	13.17	5.29	15.83
DG ECLIPSE S/250 VA	293,200	2.92	14.10	4.95	16.88
DG ECLIPSE S/250 VB	298,400	3.09	14.55	5.12	17.16
DG ECLIPSE S/250 VC	303,200	3.34	15.38	5.37	17.71
DG ECLIPSE S/250 VD	308,400	3.50	15.74	5.53	17.93
HP 1000 (45) VA	216,070	1.96	15.32	3.99	18.47
HP 1000 (45) VB	228,070	2.50	17.86	4.53	19.86
DEC VAX 11/780 VA	535,695	7.44	18.25	10.69	19.96
DEC VAX 11/780 VB	639,695	9.59	18.74	12.84	20.07
PE 3240 VA	450,995	7.13	22.17	10.38	23.02
PE 3240 VB	528,395	9.28	23.26	12.53	23.71
HARRIS 500 VA	452,770	3.78	11.69	7.03	15.53
HARRIS 500 VB	519,770	5.13	13.14	8.38	16.12
HARRIS 500 VC	531,340	5.82	14.48	9.07	17.07
HARRIS 800 VA	518,845	5.44	13.97	8.69	16.75
HARRIS 800 VB	585,845	6.79	14.88	10.04	17.14
HARRIS 800 VC	597,415	7.47	15.96	10.72	17.94
MODCOMP 7870 VA	446,345	4.04	12.75	7.29	16.33
MODCOMP 7870 VB	539,195	6.19	15.11	9.44	17.51
PRIME 750 VA	454,445	4.93	15.17	8.18	18.00
PRIME 750 VB	540,445	7.26	17.66	10.51	19.45
DG MV/8000 VA	473,890	5.08	14.75	8.33	17.58
DG MV/8000 VB	539,190	7.02	17.13	10.27	19.05
*1) SEL 32/7780 VA	435,785	6.47	N/A *1)	8.21	18.84
*1) SEL 32/7780 VB	511,750	8.29	N/A *1)	10.03	19.60
*1) SEL 32/7780 VC	597,750	8.29	N/A *1)	10.75	17.98
		*2)			

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

*1) NOT APPLICABLE SINCE P/C(HOST) FOR OTHERS DID NOT REFLECT ARRAY PROCESSOR PRICE

*2) ASSUMES BASIC OR HIGH CAPACITY API20B EXCEPT ON SEL WHERE MAP 300 WAS CHOSEN.

TABLE E-21
ARRAY PROCESSOR COST, PERFORMANCE, P/C SUMMARY

MODEL #	COST	PERFORMANCE	(P x 100,000)/C
BASIC FPS 100	\$ 76,025	9.74	12.81
BASIC AP-120B	\$ 86,595	10.16	11.73
BASIC MAP 300	\$ 93,650	7.15	7.63
BASIC MAP 300 SLOW	\$ 67,050	5.77	8.61
*1) DG IAP	\$ 16,195	3.03	18.71
HIGH CAPACITY AP-120B	\$129,445	16.24	12.54
HIGH CAPACITY VPU 3300 VC & MAP 300	\$209,720	12.28	5.86
HIGH CAPACITY VPU 3300 VA & VB	\$167,100	8.72	5.22

NOTE: *1) DG IAP CANNOT BE MAIN AP SINCE IT CAN ONLY
HAVE A MAXIMUM OF 8 KB MEMORY

TABLE E-22
ARRAY PROCESSOR PERFORMANCE STUDY

$$\text{PERFORMANCE}_{AP} = \frac{4 \times \text{MEMORY INDEX}}{\text{MEAN (MI)}} + *2)$$

$$\frac{\text{MEAN (TRFFT)}}{\text{TIME FOR REAL 1,024 POINT FFT}} +$$

$$\frac{\text{MEAN (TCFFT)}}{\text{TIME FOR COMPLEX 1,024 POINT FFT}} +$$

$$\frac{\text{MEAN (T32PC)}}{\text{TIME FOR 1,024 BY 32 POINT CONVOLUTION}} +$$

$$\frac{\text{MEAN (TCM)}}{\text{TIME FOR 1,024 POINT COMPLEX VECTOR MULTIPLY}}$$

ARRAY PROCESSOR PERFORMANCE CHARACTERISTICS

MODEL #	MI	TRFFT	TCFFT	T32PC	TCM	PERFOR-MANCE
BASIC FFS 100	1	4.0	7.13	9.9	.75	9.74
BASIC AP-120B	1	4.2	7.0	6.6	1.05	10.16
BASIC MAP 300	1	4.3	7.6	22.5	2.1	7.15
BASIC MAP 300 SLOW	1	8.0	13.6	31.5	3.0	5.77
*1) DG IAP	.063	5.6	10.8	53.7	1.6	3.03
HIGH CAPACITY AP-120B	2	2.7	4.8	6.6	.52	16.24
HIGH CAPACITY VPU 3300 VC & MAP 300	2	3.0	5.3	15.7	1.48	12.28
HIGH CAPACITY VPU 3300 VA & VB	1	3.0	5.3	15.7	1.48	8.72
MEAN	1.133	4.35	7.69	20.28	1.50	

NOTE: *1) DG IAP CANNOT BE MAIN AP SINCE IT CAN ONLY HAVE A MAXIMUM OF 8 KB MEMORY.

*2) MI IS THE MEMORY INDEX WITH 256 KB ASSIGNED THE VALUE 1.

TABLE E-23
ARRAY PROCESSOR PRICE SUMMARY
BASIC ARRAY PROCESSORS

MODEL #	DESCRIPTION	PRICE
FPS 100	DEC PDP 11/34A, 11/60, 11/70	\$ 76,025
FPS 100	DG ECLIPSE S/250	75,525
MAP 300 SLOW	DG ECLIPSE S/250 AND DEC PDP 11 SERIES	67,050
MAP 300 SLOW	HP 1000	66,550
AP-120B	DEC PDP 11/34A, 11/60, 11/70	86,595
AP-120B	DG ECLIPSE S/250 FORTRAN V	86,095
MAP 300	DG ECLIPSE S/250 AND DEC PDP 11 SERIES	93,650
MAP 300	HP 1000	93,150

HIGH CAPACITY ARRAY PROCESSORS

AP-120B	DEC VAX 11/780	\$127,945
AP-120B	DG ECLIPSE MV/8000	126,945
AP-120B	PE 3240, HARRIS 500 AND 800, SEL 32/7780, AND PRIME 750	129,445
MAP 300	PE 3240, DG MV/8000, SEL 32/7780, AND DEC VAX 11/780	209,720

TABLE E-24
BASIC FPS-100
ARRAY PROCESSOR CONFIGURATION AND PRICE

MODEL #	DESCRIPTION	PRICE
100P64	FPS-100 CONFIGURATION WITH 64 K WORDS MEMORY, 250NS	\$52,000
100TROM4	2 K WORDS ROM TABLE MEMORY	1,500
100PS4	3 K PROGRAM SOURCE MEMORY	5,500
100RTO	REAL-TIME OPTION	1,700
100IDE01 100IDG01	DEC OR DG HOST INTERFACE	3,000
100S105-X	REAL-TIME SUPERVISOR (RTS)	2,000
100PDS-X	PROGRAM DEVELOPMENT SOFTWARE	2,900
100VFC-X	VECTOR FUNCTION CHAINER	1,750
100SIG-X	SIGNAL PROCESSING LIBRARY	975
100SML-X	STANDARD MATH LIBRARY	200
100AML-X	ADVANCED MATH LIBRARY	<u>500</u>
		\$72,025
CHOOSE ONE:		
100SDE04	DEC RSX-11M, V3.2 DRIVER	\$ 4,000
100SDG01	DG RDOS/MRDOS 6.4 FORTRAN 5 DRIVER	\$ 3,500
	PRICE OF FPS 100 FOR DEC	\$76,025
	PRICE OF FPS 100 FOR DG	\$75,525

TABLE E-25
BASIC AP-120B
ARRAY PROCESSOR CONFIGURATION AND PRICE

MODEL #	DESCRIPTION	PRICE
AP120/364	AP-120B CONFIGURATION WITH 64 K WORDS 333 NS MEMORY	\$ 63,160
AP-SIGLIB	SIGNAL PROCESSING LIBRARY	975
AP-AML	ADVANCED MATH LIBRARY	500
AP-TMR	1 K WORDS RAM TABLE MEMORY	1,750
AP-TM16	2 K WORDS RAM TABLE MEMORY	1,650
AP-PS1024	1 K PROGRAM SOURCE MEMORY	3,760
AP-PR/PG	PARITY AND PAGE SELECT	4,800
AP-PDS	AP PROGRAM DEVELOPMENT SOFTWARE	<u>3,000</u>
		\$ 79,595
CHOOSE ONE:		
AP-DE01-I AP-DG01-I	DEC OR DG HOST INTERFACE	\$ 3,000
AP-HP01-I	HEWLETT PACKARD HOST INTERFACE	\$ 4,000
AP-HA01-I AP-ID01-I AP-PRO1-I AP-SE01-I	HARRIS, INTERDATA, PRIME, SEL HOST INTERFACE	\$ 5,000
CHOOSE ONE:		
AP-DG01-S	DG RDOS/MRDOS FORTRAN V DRIVER	\$ 3,500
AP-DG02-S AP-DE04-S AP-HP01-S	DG RDOS/MRDOS FORTRAN IV, DEC RSX-11M, HP RTE IV DRIVER	\$ 4,000
AP-ID01-S AP-HA02-S AP-PRO1-S AP-SE01-S	INTERDATA 05/32 MT, HARRIS VULCAN, PRIME PRIMOS, SEL RTM DRIVER	\$ 4,500
	PRICE OF AP120B FOR DEC	\$ 86,595
	PRICE OF AP120B FOR DG FORTRAN V	\$ 86,095
	PRICE OF AP120B FOR DG FORTRAN IV	\$ 86,595
	PRICE OF AP120B FOR INTERDATA, HARRIS, PRIME, SEL	\$ 89,095
	PRICE OF AP120B FOR HEWLETT PACKARD	\$ 88,095

TABLE E-26
BASIC MAP 300 (COMPARABLE TO BASIC AP120-B)
ARRAY PROCESSOR CONFIGURATION AND PRICE

MODEL #	DESCRIPTION	PRICE
1033	MAP 300 PROCESSOR, 105 AMP POWER SUPPLY, 23 SLOT CHASSIS	\$ 20,400
7180	75 AMP AUXILIARY POWER SUPPLY	1,000
2520	64 KB 500 NS PROGRAM MEMORY	7,500
(4) 2204	64K 300 NS DATA MEMORY	51,600
RSX/N 8300-32MT/N RTE/N RDOS/N	SNAP II SOFTWARE WITH STANDARD ARRAY FUNCTION LIBRARY	3,000
RSX 8510-32MT RTE RDOS	EXTENDED ARRAY FUNCTION LIBRARY II	1,200
RSX 8000-32MT RTE RDOS	MAP DEVELOPMENT SOFTWARE	1,200
9500	MAP INSTALLATION	1,000
7140	PROGRAMMER'S PANEL	1,750
CHOOSE ONE:		
8901-RSX	DEC RSX-11M DRIVER	1,500
8910-RDOS	DG RDOS DRIVER	1,500
8920-RTE	HP RTE IV DRIVER	1,500
8940-32MT	INTERDATA OS/32 MT DRIVER	<u>1,500</u>
		\$ 90,150
CHOOSE ONE:		
3110 3300 3400 3420	DEC PDP-11 UNIBUS, INTERDATA, DG, SEL INTERFACE	\$ 3,500
3200	HP 21 MX INTERFACE	\$ 3,000
	PRICE OF MAP 300 FOR INTERDATA, DG, SEL, DEC	\$ 93,650
	PRICE OF MAP 300 FOR HP	\$ 93,150

TABLE E-27
 BASIC MAP 300 (SLOW, EXCEPTION SINCE NO FPS EQUAL)
 ARRAY PROCESSOR CONFIGURATION AND PRICE

MODEL #	DESCRIPTION	PRICE
1053	MAP 300 CONFIGURATION WITH 64 K WORDS 500 NS MEMORY FOR DATA, 64 K BYTES 500 NS MEMORY FOR PROGRAM, AND 16 K BYTES 170 NS MEMORY, SNAP II SOFTWARE AND LIBRARY	\$ 55,900
7180	75 AMP AUXILARY POWER SUPPLY	1,000
7140	PROGRAMMER'S PANEL	1,750
9500	MAP INSTALLATION	1,000
RSX 8000-32MT RTE RDOS	MAP DEVELOPMENT SOFTWARE	1,200
RSX 8510-32MT RTE RDOS	EXTENDED ARRAY FUNCTION LIBRARY II	1,200
CHOOSE ONE:		
8901-RSX	DEC RSX-11M DRIVER	\$ 1,500
8910-RDOS	DG RDOS DRIVER	\$ 1,500
8920-RTE	HP RATE IV DRIVER	\$ 1,500
8940-32MT	INTERDATA OS/32 MT DRIVER	\$ 1,500
		\$ 63,550
CHOOSE ONE:		
3110	DEC PDP-11 UNIBUS INTERFACE	\$ 3,500
3200	HP 21MX INTERFACE	\$ 3,000
3300 3400 3420	INTERDATA, DG, SEL INTERFACE	\$ 3,500
	PRICE OF MAP 300 FOR INTERDATA, DG, SEL, DEC	\$ 67,050
	PRICE OF MAP 300 FOR HP	\$ 66,550

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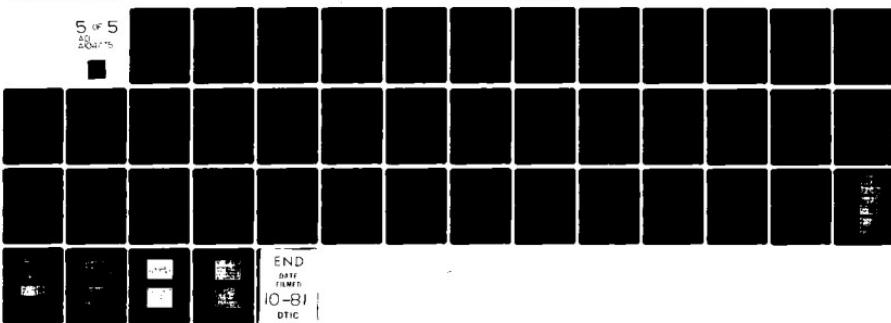
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TABLE E-28
HIGH CAPACITY AP-120B
ARRAY PROCESSOR CONFIGURATION AND PRICE

MODEL #	DESCRIPTION	PRICE
AP-120/6128	AP120B CONFIGURATION WITH 128K WORDS 167NS MEMORY	\$ 91,610
AP-SIGLIB	SIGNAL PROCESSING LIBRARY	975
AP-AML	ADVANCED MATH LIBRARY	500
AP-TMR	1 K WORDS RAM TABLE MEMORY	1,750
AP-TM16	2 K WORDS RAM TABLE MEMORY	1,650
AP-PS1024	1 K PROGRAM SOURCE MEMORY	3,760
AP-PAR	PARITY ON MEMORY	3,100
AP-PDS	AP PROGRAM DEVELOPMENT SOFTWARE	3,000
(2) AP-GPICP	GENERAL PURPOSE INPUT/OUTPUT PROCESSOR (INTERFACES): GPIOPS	13,600
		\$119,945
CHOOSE ONE:		
AP-DE01-I AP-DG01-I	DEC OR DG HOST INTERFACE	\$ 3,000
AP-HA01-I AP-ID01-I AP-PRO1-I AP-SE01-I	HARRIS, INTERDATA, PRIME, SEL HOST INTERFACE	\$ 5,000
CHOOSE ONE:		
AP-DG02-S	DG RDOS/MRDOS FORTRAN IV	\$ 4,000
AP-DE06	DEC VMS DRIVER	\$ 5,000
AP-ID01-S AP-HA02-S AP-PRO1-S AP-SE01-S	INTERDATA 05/32 MT, HARRIS VULCAN, PRIME PRIMOS, SEL RTM DRIVER	\$ 4,500
	PRICE OF AP120B FOR DEC VMS	\$127,945
	PRICE OF AP120B FOR DG	\$126,945
	PRICE OF AP120B FOR INTERDATA, HARRIS, PRIME, SEL	\$129,445

TABLE E-29
HIGH CAPACITY MAP 300
ARRAY PROCESSOR CONFIGURATION AND PRICE

MODEL #	DESCRIPTION	PRICE
1033	MAP 300 PROCESSOR, 105 AMP POWER SUPPLY, 23 SLOT CHASSIS	\$ 20,400
7180	75 AMP AUXILIARY POWER SUPPLY	1,000
2520	64 KB 500 NS PROGRAM MEMORY	7,500
(8) 2440	64 KB 170 NS DATA MEMORY	159,920
RSX/N 8300-32MT/N RTE/N RDOS/N	SNAP II SOFTWARE WITH STANDARD ARRAY FUNCTION LIBRARY	3,000
RSX 8510-32MT RTE RDOS	EXTENDED ARRAY FUNCTION LIBRARY II	1,200
RSX 8000-32MT RTE RDOS	MAP DEVELOPMENT SOFTWARE	1,200
(2) 4070	IOS-4 INPUT/OUTPUT SCROLL INTERFACES	7,000
9500	MAP INSTALLATION	1,000
7140	PROGRAMMER PANEL	1,750
RSX 8400-32MT RTE RDOS	I/O SCROLL SUPPORT PACKAGE	750
CHOOSE ONE:		
8901-RSX	DEC VAX VMS DRIVER	1,500
8910-RDOS	DG RDOS DRIVER	1,500
8920-RTE	HP RTE IV DRIVER	1,500
8940-32MT	INTERDATA OS/32 MT DRIVER	<u>1,500</u>
		\$206,220
CHOOSE ONE:		
3111 3300 3400 3420	DEC VAX UNIBUS, INTERDATA, DG, SEL INTERFACE	\$ 3,500
	PRICE OF MAP 300 FOR INTERDATA, DG, SEL, DEC	\$209,720

TABLE E-30
BASIC HOST COST, PERFORMANCE, P/C SUMMARY

MODEL #	COST	PERFOR-MANCE	(P x 1,000,000)/C
DEC PDP 11/34A VA	\$125,330	1.47	11.73
DEC PDP 11/34A VB	143,630	1.66	11.56
DEC PDP 11/60 VA	158,580	1.66	10.47
DEC PDP 11/60 VB	176,880	1.85	10.46
DEC PDP 11/70 VA	208,680	2.38	11.41
DEC PDP 11/70 VB	247,580	3.26	13.17
DG ECLIPSE S/250 VA	207,105	2.92	14.10
DG ECLIPSE S/250 VB	212,305	3.09	14.55
DG ECLIPSE S/250 VC	217,105	3.34	15.38
DG ECLIPSE S/250 VD	222,305	3.50	15.74
HP 1000 (45) VA	127,975	1.96	15.32
HP 1000 (45) VB	139,975	2.50	17.86

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

TABLE E-31
HIGH CAPACITY HOST COST, PERFORMANCE, P/C SUMMARY

MODEL #	COST	PERFOR-MANCE	(P x 1,000,000)/C
DEC VAX 11/780 VA	\$407,750	7.44	18.25
DEC VAX 11/780 VB	511,750	9.59	18.74
PE 3240 VA	321,550	7.13	22.17
PE 3240 VB	398,950	9.28	23.26
HARRIS 500 VA	323,325	3.78	11.69
HARRIS 500 VB	390,325	5.13	13.14
HARRIS 500 VC	401,895	5.82	14.48
HARRIS 800 VA	389,400	5.44	13.97
HARRIS 800 VB	456,400	6.79	14.88
HARRIS 800 VC	467,970	7.47	15.96
MODCOMP 7870 VA	316,900	4.04	12.75
MODCOMP 7870 VB	409,750	6.19	15.11
PRIME 750 VA	325,000	4.93	15.17
PRIME 750 VB	411,000	7.26	17.66
DG MV/8000 VA	344,445	5.08	14.75
DG MV/8000 VB	409,745	7.02	17.13
*1) SEL 32/7780 VA	435,785	6.47	N/A *2)
*1) SEL 32/7780 VB	511,750	8.29	N/A *2)
*1) SEL 32/7780 VC	597,750	8.29	N/A *2)

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

*1) UNLIKE OTHERS, SEL PRICES INCLUDES MAP 300 ARRAY PROCESSOR PRICE.

*2) NOT APPLICABLE SINCE OTHER PRICES DO NOT REFLECT ARRAY PROCESSOR PRICE.

TABLE E-32
BASIC AND HIGH CAPACITY HOST PERFORMANCE STUDY

PERFORMANCE HOST = MILLION OPERATIONS PER SECOND +
 MEAN (MOPS)

MEMORY INDEX +
 MEAN (MI)

ARRAY PROCESSOR BUS INTERFACE RATE +
 MEAN (APBIR)

HOST BUS RATE +
 MEAN (HBR)

TOTAL DISK STORAGE
 MEAN (DISK)

NOTE: MI IS THE MEMORY INDEX WITH 256 KB ASSIGNED THE VALUE 1.

TABLE E-33
BASIC HOST PERFORMANCE CHARACTERISTICS

MODEL #	MOPS	MI	APBIR	HBR	DISK	PERFOR-MANCE
DEC PDP 11/34A VA	.05	1	1.5	1.5	134	1.47
DEC PDP 11/34A VB	.05	1	1.5	1.5	243	1.66
DEC PDP 11/60 VA	.09	1	1.5	1.5	134	1.66
DEC PDP 11/60 VB	.09	1	1.5	1.5	243	1.85
DEC PDP 11/70 VA	.12	2	1.5	3.5	243	2.38
DEC PDP 11/70 VB	.12	4	1.5	3.5	512	3.26
DG ECLIPSE S/250 VA	.128	2	~1.5	6.6	373	2.92
DG ECLIPSE S/250 VB	.128	2	~1.5	6.6	467	3.09
DG ECLIPSE S/250 VC	.128	4	~1.5	6.6	373	3.34
DG ECLIPSE S/250 VD	.128	4	~1.5	6.6	467	3.50
HP 1000 (45) VA	.074	2	1.6	2.2	170	1.96
HP 1000 (45) VB	.074	4	1.6	2.2	240	2.50
*1) MEAN	.209	4.79	2.31	11.07	575.6	
		*2)	*3)			

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

*1) MEAN IS ALWAYS CALCULATED FROM ALL BASIC AND HIGH CAPACITY HOSTS.

*2) MI IS THE MEMORY INDEX WITH 256 KB ASSIGNED THE VALUE 1.

*3) ~ MEANS UNMEASURED ESTIMATE.

TABLE E-34
HIGH CAPACITY HOST PERFORMANCE CHARACTERISTICS

MODEL #	MOPS	MT	APBIR	HBR	DISK	PERFOR-MANCE
DEC VAX 11/780 VA	.30	4	8.1	13.3	268	7.44
DEC VAX 11/780 VB	.30	8	8.1	13.3	1,024	9.59
PE 3240 VA	.319	4	1.6	40	268	7.13
PE 3240 VB	.319	8	1.6	40	1,024	9.28
HARRIS 500 VA	.20	4.5	≈ 1.6	7.9	276	3.78
HARRIS 500 VB	.20	4.5	≈ 1.6	7.9	1,052	5.13
HARRIS 500 VC	.20	4.5	≈ 1.6	7.9	1,447	5.82
HARRIS 800 VA	.35	9	≈ 1.6	7.9	276	5.44
HARRIS 800 VB	.35	9	≈ 1.6	7.9	1,052	6.79
HARRIS 800 VC	.35	9	≈ 1.6	7.9	1,447	7.47
MODCOMP 7870 VA	.258	4	1.8	8	268	4.04
MODCOMP 7870 VB	.258	8	1.8	8	1,024	6.19
PRIME 750 VA	.24	4	4	7.5	308	4.93
PRIME 750 VB	.24	8	4	7.5	1,168	7.26
DG MV/8000 VA	.26	4	≈ 1.6	18.2	384	5.08
DG MV/8000 VB	.26	8	≈ 1.6	18.2	1,021	7.02
*1) SEL 32/7780 VA	.30	4	3.2	26	268	6.47
*1) SEL 32/7780 VB	.30	8	3.2	26	835	8.29
*1) SEL 32/7780 VC	.30	8	3.2	26	835	8.29
*2) MEAN	.209	4.79	2.31	11.07	575.6	
			*3)			

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

*1) UNLIKE OTHERS, SEL PRICES INCLUDES MAP 300 ARRAY PROCESSOR PRICE.

*2) MEAN IS ALWAYS CALCULATED FROM ALL BASIC AND HIGH CAPACITY HOSTS.

*3) ≈ MEANS UNMEASURED ESTIMATE.

TABLE E-35
BASIC HOST PRICE SUMMARY

MODEL #	PRICE
DEC PDP 11/34A VA	\$125,330
DEC PDP 11/34A VB	143,630
DEC PDP 11/60 VA	158,580
DEC PDP 11/60 VB	176,880
DEC PDP 11/70 VA	208,680
DEC PDP 11/70 VB	247,580
DG ECLIPSE S/250 VA	207,105
DG ECLIPSE S/250 VB	212,305
DG ECLIPSE S/250 VC	217,105
DG ECLIPSE S/250 VD	222,305
HP 1000 (45) VA	127,975
HP 1000 (45) VB	139,975

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

TABLE E-36
HIGH CAPACITY HOST PRICE SUMMARY

MODEL #	PRICE
DEC VAX 11/780 VA	\$407,750
DEC VAX 11/780 VB	511,750
PE 3240 VA	321,550
PE 3240 VB	398,950
HARRIS 500 VA	323,325
HARRIS 500 VB	390,325
HARRIS 500 VC	401,895
HARRIS 800 VA	389,400
HARRIS 800 VB	456,400
HARRIS 800 VC	467,970
MODCOMP 7870 VA	316,900
MODCOMP 7870 VB	409,750
PRIME 750 VA	325,000
PRIME 750 VB	411,000
DG MV/8000 VA	344,445
DG MV/8000 VB	409,745
*1) SEL 32/7780 VA	435,785
*1) SEL 32/7780 VB	511,750
*1) SEL 32/7780 VC	597,750

NOTE: VA STANDS FOR VERSION A, VB STANDS FOR VERSION B, ETC.

*1) UNLIKE OTHERS, SEL PRICES INCLUDES MAP 300 ARRAY
PROCESSOR PRICE

TABLE E-37
 MDC (NASA) BENCHMARK TESTS OF COMPUTERS - KOPBM, MOPS
 HOST BASIC CANDIDATES

MANUFACTURER	MODEL	MILLIONS OF OPERATIONS PER SECOND
RAYTHEON	704	.0294
DEC	PDP 11/45	.03
IBM	370/135 (VM)	.037
HP	3000A	.041
RAYTHEON	500	.042
DEC	PDP 11/34A, FFP	.05
TANDEM	T/16	.067
HP	1000	.074
HONEYWELL	6031	.08
IBM	370/148 (VM)	.088
DEC	PDP 11/60, FFP	.09
DEC	PDP 11/70	.12
DATA GENERAL	S/250, FFP	.128

TABLE E-38
 MDC (NASA) BENCHMARK TESTS OF COMPUTERS - KOPBM, MOPS
 HOST HIGH CAPACITY CANDIDATES

MANUFACTURER	MODEL	MILLIONS OF OPERATIONS PER SECOND
HARRIS	SYSTEM 135	.11
SEL	32/77	.15
PERKIN ELMER	3220	.16
HARRIS	SYSTEM 300	.16
SEL	32/75	.17
CDC	6400	.17
INTERDATA (PERKIN ELMER)	8/32	.19
HARRIS	SYSTEM 500	.20
PRIME	750	.24
SEL	32/7780 (2500)	.25 = 2 x .127
MODCOMP	7860, 7870	.258
DATA GENERAL	MV 8000	.26
SEL	32/7780 (2510)	.27 = 2 x .136
DEC	VAX 11/780	.30
SEL	32/7780 (2520, 2530, 2531)	.30 = 2 x .151
INTERDATA (PERKIN ELMER)	3240	.319
HARRIS	800	.35
CDC	6600	.45
IBM	370/168	.7178
CDC	CYBER 175	1.16
IBM	3033	1.5135

TABLE E-39
BASIC HOST CONFIGURATION AND PRICE
DEC PDP 11/34A VERSIONS A AND B

MODEL #	DESCRIPTION	PRICE
SM-30UVB-CA	PDP 11/34A CONFIGURATION WITH 256 KB MEMORY, RSX-11M OPERATING SYSTEM, 67 MB RM02 DISK DRIVE WITH CONTROLLER, TE16 TAPE DRIVE WITH CONTROLLER	\$ 75,500
KK11-A	2KB CACHE	4,150
FP11-A	FLOATING POINT PROCESSOR	3,100
KW11-K	REAL TIME CLOCK	1,050
QP100-AM	FORTRAN IV PLUS	5,800
QP301-AM	DATATRIEVE-11 AND RMS-11K DATA MANAGEMENT SYSTEM	4,500
QP602-AM	SORT-11	430
QJ918-AM	BASIC PLUS II	<u>5,100</u>
CHOOSE ONE:		\$ 99,630
RJM02-AA	RM02 DISK DRIVE AND CONTROLLER - 67MB	25,700
RJP06-AA	RP06 DISK DRIVE AND CONTROLLER - 176MB	44,000
	PRICE OF DEC PDP 11/34A VERSION A (2 67MB DISKS)	\$125,330
	PRICE OF DEC PDP 11/34A VERSION B (176MB & 67 MB DISKS)	\$143,630

TABLE E-40
BASIC HOST CONFIGURATION AND PRICE
DEC PDP 11/60 VERSIONS A & B

MODEL #	DESCRIPTION	PRICE
SM-60UVB-CA	PDP 11/60 CONFIGURATION WITH 256 KB MEMORY, RXS-11M OPERATING SYSTEM, 2 KB CACHE, 67 MB RM02 DISK DRIVE WITH CONTROLLER, TE16 TAPE DRIVE WITH CONTROLLER	\$ 88,800
RK71I-EA	28 MB RK07 DISK DRIVE AND CONTROLLER	15,500
KU116-AV	USER CONTROL STORE AND SOFTWARE	5,700
FP11-EA	FLOATING POINT PROCESSOR	6,000
KW11-K	REAL TIME CLOCK	1,050
QP100-AM	FORTRAN IV PLUS	5,800
QP301-AM	DATATRIEVE-11 AND RMS-11K DATA MANAGEMENT SYSTEM	4,500
QP602-AM	SORT-11	430
QJ918-AM	BASIC PLUS II	<u>5,100</u>
		\$132,880
CHOOSE ONE:		
RJM02-AA	RM02 DISK DRIVE AND CONTROLLER - 67 MB	25,700
RJP06-AA	RP06 DISK DRIVE AND CONTROLLER - 176 MB	44,000
	PRICE OF DEC PDP 11/60 VERSION A (TWO 67MB DISKS)	\$158,580
	PRICE OF DEC PDP 11/60 VERSION B (176 MB AND 67 MB DISKS)	\$176,880

TABLE E-41
BASIC HOST CONFIGURATION AND PRICE
DEC PDP 11/70 VERSIONS A & B

MODEL #	DESCRIPTION	PRICE
CHOOSE ONE:		
SN-70-TVA-CA	PDP 11/70 CONFIGURATION WITH 512 KB MEMORY, RSX-11M PLUS OPERATING SYSTEM, 2 KB CACHE, 67 MB RM03 DISK DRIVE WITH CONTROLLER, TE 16 TAPE DRIVE WITH CONTROLLER	\$139,100
SN-70DBA-CA	PDP 11/70 CONFIGURATION WITH 1024 KB MEMORY, RSX-11M PLUS OPERATING SYSTEM, 2 KB CACHE, 256 MB FORMATTED RM05 DISK DRIVE WITH CONTROLLER, TU77 TAPE DRIVE WITH CONTROLLER	\$178,000
FP11-C	FLOATING POINT PROCESSOR	6,000
KW11-K	REAL TIME CLOCK	1,050
QJ688-AM	FORTRAN IV PLUS	5,800
QP301-AM	DATATRIEVE-11 AND RMS-11 K DATA MANAGEMENT SYSTEM	4,500
QP602-AM	SORT - 11	430
QR514-AM	BASIC PLUS II	5,100
QJ715-AM	FMS-11 FORMS MANAGEMENT SYSTEM	<u>2,700</u>
		\$ 25,580
CHOOSE ONE:		
RJP06-AA (SM-70TVB-CA)	RP06 DISK DRIVE AND CONTROLLER - 176 MB	44,000
RWM05-AA (SM-70DBA-CA)	RM05 DISK DRIVE AND CONTROLLER - 256 MB	44,000
	PRICE OF DEC PDP 11/70 VERSION A (67 MB AND 176 MB DISKS)	\$208,680
	PRICE OF DEC PDP 11/70 VERSION B (TWO 256 MB FORMATTED DISKS)	\$247,580

TABLE E-42
DATA GENERAL ECLIPSE S/250
BASIC HOST CONFIGURATION AND PRICE

MODEL #	DESCRIPTION	PRICE
CHOOSE ONE:		
8635-R8	ECLIPSE S/250 WITH 4 WAY INTERLEAVED 512 KB MEMORY	\$ 49,500
8635-VA	ECLIPSE S/250 WITH 4 WAY INTERLEAVED 1024 KB MEMORY	\$ 59,500
4241	ULM-5 4 LINE ASYNC. MUX SUBSYSTEM	1,400
6026	MAGNETIC TAPE SUBSYSTEM	15,500
8638	WRITABLE CONTROL STORE	4,200
8641	FLOATING POINT PROCESSOR	6,195
8639	CHARACTER INSTRUCTION SET	1,575
8644	INTEGRAL ARRAY PROCESSOR	14,595
(2) 8648	MEMORY I/O SYSTEM MODULE 8 SLOTS	1,890
8650-A	PERIPHERAL BAY	1,300
8651-A	EXPANSION BAY	6,500
8649	BOOSTER POWER SUPPLY	3,500
8642	BURST MULTIPLEXER CHANNEL	3,150
4065	I/O INTERFACE FOR 4068	200
4191	I/O INTERFACE FOR 4068	400
4068	PROGRAMMABLE INTERVAL TIMER	600
		\$ 61,005
CHOOSE ONE PAIR:		
6060	96 MB DISK SUBSYSTEM AND CONTROLLER	25,800
6122	277 MB DISK SUBSYSTEM AND CONTROLLER	38,500
6061	190 MB DISK SUBSYSTEM AND CONTROLLER	31,000
6122	277 MB DISK SUBSYSTEMS AND CONTROLLERS	38,500
3803	FORTRAN COMMERCIAL SUBROUTINE PACKAGE	100
3804-02H	DATAPLOT FORTRAN PLOTTING SUBROUTINES	100
3804-30H	DATAPLOT FORTRAN PLOTTING SUBROUTINES SOURCE	200
3604-24R	DTOS DIAGNOSTICS FICHE	25
3605-24R	DTOS PERIPHERAL DIAGNOSTICS FICHE	25
3625-00H	AOS OPERATING SYSTEM	4,000
3625-30H	AOS OPERATING SYSTEM SOURCE	10,000
3627-00H	FORTRAN V	3,000
3632-01H	SORT/MERGE AND COPY UTILITIES	750
3633-00H	INFOS II FILE MANAGEMENT SYSTEM	2,500
3637-01H	INFOS II QUERY LANGUAGE	2,000
3730-02H	WCS MICRO ASSEMBLER AND LOADER	100
3738-01H	ARRAY PROCESSOR SOFTWARE (IAP)	1,100
3738-30H	ARRAY PROCESSOR SOURCE (IAP)	500
3819-02H	MACRO PROCESSOR FOR HIGH LEVEL LANGUAGES	1,000
3628-00H	BASIC (EXTENDED)	1,200
3717-02H	DG/L SYSTEM LANGUAGE	5,700
		\$ 32,300
	PRICE OF DG ECLIPSE S/250 VERSION A (RB-512KB, 96 AND 277 MB)	\$207,105
	PRICE OF DG ECLIPSE S/250 VERSION B (RB-512KB, 190 AND 277 MB)	\$212,305
	PRICE OF DG ECLIPSE S/250 VERSION C (VA-1,024 KB, 96 AND 277 MB)	\$217,105
	PRICE OF DG ECLIPSE S/250 VERSION D (VA-1,024 KB, 190 AND 277 MB)	\$222,305

TABLE E-43
BASIC HOST CONFIGURATION AND PRICE
HP 1000 MODEL 45 VERSIONS A AND B

MODEL #	DESCRIPTION	PRICE
2177C	HP 1000 MODEL 45 SYSTEM CONFIGURATION	\$ 46,000
OPTION 002	CABINET BAY	1,850
OPTION 014	CREDIT MEMORY AND CONTROLLER, 128 KB	-5,500
OPTION 019	CREDIT CONSOLE, 20 MB DISK AND CONTROLLER	-22,490
12990B	MEMORY EXTENDER	4,500
(2) 13197A	1 KW WRITABLE CONTROL STORE	4,000
92061A	WCS SOFTWARE	1,000
OPTION 020	MINI CARTRIDGE FOR ABOVE	0
2648A	GRAPHICS CONSOLE	5,950
OPTION 007	MINI CARTRIDGE I/O	1,600
OPTION 032	EXTENDED ASYNC COMMUNICATION	150
7970B	800 BPI, 9 TRACK, 45 IPS TAPE DRIVE	6,870
OPTION 236	RACK MOUNT FOR TAPE AND INTERFACE CARDS	2,630
(2) 13175B	MAC DISK INTERFACE	1,400
2635B	PRINTING TERMINAL	3,950
OPTION 051	264X EDGE CONNECTOR	65
92832A	PASCAL LANGUAGE	4,000
OPTION 050	800 BPI TAPE FOR ABOVE	0
92101A	BASIC LANGUAGE	1,000
OPTION 020	MINI CARTRIDGE FOR ABOVE	0
92069A	IMAGE DATABASE MANAGEMENT SYSTEM	3,000
OPTION 020	MINI CARTRIDGE FOR ABOVE	0
92068X	RTE IV B OPERATING SYSTEM SOURCE	15,000
OPTION 050	800 BPI TAPE FOR ABOVE	0
92062X	RTE IV B DRIVER SOURCES	1,000
OPTION 050	800 BPI TAPE FOR ABOVE	0
CHOOSE ONE PAIR:		
7920M	50 MB DISK DRIVE	18,000
7925M	120 MB DISK DRIVE	21,000
7925M	120 MB DISK DRIVE	21,000
7925M	120 MB DISK DRIVE	21,000
CHOOSE ONE:		
12788C	512 KB MEMORY	13,000
12788D	1,024 KB MEMORY	22,000
PRICE OF HP 1000 VERSION A (512 KB, 50 AND 120 MB DISKS)		\$127,975
PRICE OF HP 1000 VERSION B (1,024 KB, TWO 120 MB DISKS)		\$139,975

TABLE E-44
HIGH CAPACITY HOST CONFIGURATION AND PRICE
DEC VAX 11/780 VERSION A
(1 MB INTERLEAVED MEMORY, 268 MB DISK TOTAL)

MODEL #	DESCRIPTION	PRICE
SV-AXTBA-CA	VAX 11/780 CONFIGURATION WITH 512 KB MEMORY, 8 KB CACHE, 12 KB WRITABLE DIAGNOSTIC CONTROL STORE, REAL-TIME CLOCK, TIME OF YEAR CLOCK, 67 MB RM03 DISK DRIVE WITH CONTROLLER, TU77 TAPE DRIVE WITH CONTROLLER	\$185,000
FP-780-AA	FLOATING POINT PROCESSOR	10,600
KU780-YY	USER WRITABLE CONTROL STORE - 12 KB	10,700
MS780-CC	512 KB MEMORY WITH CONTROLLER	26,600
DW780-AA	UNIBUS ADAPTER	12,300
DR780-AA	SBI ADAPTER	18,700
LPA11-K	LABORATORY DIRECT MEMORY ACCESS CONTROLLER	5,300
KW11-K	REAL-TIME CLOCK	1,050
H9602-HA	CPU EXPANSION CABINET	4,250
(2) REM03-AA	TWO RM03 DISK DRIVES AND CONTROLLERS - 67 MB	53,600
RM03-AA	RM03 DISK DRIVE	20,300
QE106-AY	BLISS - 32 SYSTEM LANGUAGE	13,800
QE100-AY	FORTRAN IV PLUS LANGUAGE	5,800
QE001-AM	VMS OPERATING SYSTEM	13,800
QE102-AY	BASIC PLUS II LANGUAGE	5,100
QE105-AY	DATATRIEVE (DATA MANAGEMENT SERVICES)	2,600
MD-VAX	DIAGNOSTIC SOURCE	3,000
MD-VAX-R	ONE YEAR DIAGNOSTIC UPDATE	1,800
ZE014-CY	USER DIAGNOSTIC SOURCE	1,150
QE001-MM	VMS SOURCE	11,500
	PRICE OF DEC VAX 11/780 VERSION A	\$407,750

TABLE E-45
HIGH CAPACITY HOST CONFIGURATION AND PRICE
DEC VAX 11/780 VERSION B
(2 MB INERLEAVED MEMORY, 1024 MB DISK TOTAL)

MODEL #	DESCRIPTION	PRICE
SV-AXDBA-CA	VAX 11/780 CONFIGURATION WITH 1,024 KB MEMORY, 8 KB CACHE, 12 KB WRITABLE DIAGNOSTIC CONTROL STORE, REAL-TIME CLOCK, TIME OF YEAR CLOCK, 256 MB FORMATTED RM05 DISK DRIVE WITH CONTROLLER, TU77 TAPE DRIVE WITH CONTROLLER	\$227,800
FP-780-AA	FLOATING POINT ACCELERATOR	10,600
KU780-YY	USER WRITABLE CONTROL STORE - 12 KB	10,700
MS780-CC	512 KB MEMORY WITH CONTROLLER	26,600
MS780-DB	512 KB MEMORY	13,900
DW780-AA	UNIBUS ADAPTER	12,300
DR780-AA	SBI ADAPTER	18,700
LP411-K	LABORATORY DIRECT MEMORY ACCESS CONTROLLER	5,300
KW11-K	REAL-TIME CLOCK	1,050
H9602-HA	CPU EXPANSION CABINET	4,250
(2) REM05-AA	TWO RM05 DISK DRIVES AND CONTROLLERS - 256 FORMATTED MB EACH	38,000
RM05-AA	RM05 DISK DRIVE	34,000
QE106-AY	BLISS - 32 SYSTEM LANGUAGE	13,800
QE100-AY	FORTRAN IV PLUS LANGUAGE	5,800
QE001-AM	VMS OPERATING SYSTEM	13,800
QE102-AY	BASIC PLUS II LANGUAGE	5,100
QE105-AY	DATATRIEVE (DATA MANAGEMENT SERVICES)	2,600
MD-VAX	DIAGNOSTIC SOURCE	3,450
MD-VAX-R	ONE YEAR DIAGNOSTIC UPDATE	2,070
ZE014-CY	USER DIAGNOSTIC SOURCE	1,150
QE001-MM	VMS SOURCE	11,500
	PRICE OF VAX 11/780 VERSION B	\$511,750

TABLE E-46
HIGH CAPACITY HOST CONFIGURATION AND PRICE
PERKIN ELMER INTERDATA 3240

MODEL #	DESCRIPTION	PRICE
CHOOSE ONE:		
M32-482	3242 BASIC CONFIGURATION WITH 1 MB MEMORY, CACHE, FFP, 2 KW WRITABLE CONTROL STORE, 2 WAY INTERLEAVING, 75 IPS TAPE DRIVE AND CONTROLLER, 67 MB DISK DRIVE AND CONTROLLER	\$187,000
M32-484	SAME AS M32-482 EXCEPT WITH 300 MB DISK INSTEAD OF 67 MB DISK AND WITH 2 MB MEMORY TOTAL	223,900
M32-430		
M32-429	MEMORY EXPANSION CHASSIS	3,500
M32-404	MEMORY EXPANSION UNIT, 4 WAY INTERLEAVING	15,000
(3) M32-421	DMA BUS EXPANSION	15,000
M48-061	3240 CLOCK MODULE	900
	OS/32 SOURCE	5,000
S80-016-ABC	OS/32 OPERATING SYSTEM	6,000
S80-017-ABC	OS/32 MULTI-USER OPERATING SYSTEM	2,800
S80-020-ABC	OS/32 TEXT UTILITY	1,100
S80-022-ABC	DMS/32 DATA MANAGEMENT SERVICES	6,000
S80-216-ABC	FORTRAN VII	6,000
S90-408-71	SORT/MERGE II	1,100
S90-028-71	FORTRAN ENHANCEMENT PACKAGE	600
S90-210-71	BASIC II DPFP	450
S90-406-71	WCS DEVELOPMENT SYSTEM	<u>600</u>
		\$ 64,050
CHOOSE ONE:		
(3) M46-600	MSM 80 DISK SYSTEM, 67 MB DISK AND CONTROLLER	70,500
(3) M46-604	MSM 300 DISK SYSTEM, 256 MB DISK AND CONTROLLER	111,000
	PRICE OF PERKIN ELMER 3240 VERSION A	\$321,550
	PRICE OF PERKIN ELMER 3240 VERSION B	\$398,950

TABLE E-47
HIGH CAPACITY CONFIGURATION AND PRICE
HARRIS SYSTEM 500 VERSIONS A, B, AND C

MODEL #	DESCRIPTION	PRICE
H500	192 KB SYSTEM 500 PACKAGE	\$ 99,600
001D	960 KB MEMORY	19,400
073	MEMORY EXPANSION UNIT	7,500
074	EXTENDED MEMORY KIT	2,000
(4) 047	UNIVERSAL BLOCK CHANNELS	13,200
071	I/O EXPANSION UNIT	6,800
015B	SCIENTIFIC ARITHMETIC UNIT	10,395
022	REAL TIME CLOCK	1,750
051	PRIORITY INTERRUPT	3,675
6890A	75 IPS TAPE DRIVE WITH CONTROLLER	24,600
1150	VULCAN OPERATING SYSTEM SOURCE	3,000
1310	SORT/MERGE	300
9815014-418	H500 DIAGNOSTICS SOURCE	300
9810126-108	DIAGNOSTIC SUPPORT LIBRARY	75
101	DIAGNOSTIC SUPPORT LIBRARY SOURCE	100
104	DIAGNOSTIC SUPPORT LIBRARY INSTRUCTIONS	5
118	DIAGNOSTIC SUPPORT LIBRARY LISTINGS	25
1411	FORTRAN 77	7,500
1415	FORTRAN LOAD AND GO	500
1431	EXTENDED BASIC	5,000
1720	TX TEXT EDITOR	250
1710	FORMAT LISTING UTILITY	250
1530	AZ7 QUERY LANGUAGE AND REPORT WRITER	9,500
		\$215,725
CHOOSE ONE:		
(4) 5530-C	69 MB DISKS AND CONTROLLERS	107,600
(4) 5550-C	263 MB DISKS AND CONTROLLERS	174,600
(1) & (2) 5550-C	263 MB DISK AND CONTROLLER	186,170
5660	592 MB DISKS AND CONTROLLERS (5660 NON-REMOVABLE)	
	PRICE OF HARRIS SYSTEM 500 VERSION A (276 MB)	\$323,325
	PRICE OF HARRIS SYSTEM 500 VERSION B (1052 MB)	\$390,325
	PRICE OF HARRIS SYSTEM 500 VERSION C (1447 MB)	\$401,895

TABLE E-48

HIGH CAPACITY CONFIGURATION AND PRICE
HARRIS SYSTEM 800 VERSIONS A, B, AND C

MODEL #	DESCRIPTION	PRICE
H800	384 KB SYSTEM 800 PACKAGE	\$165,900
001E	1,920 KB MEMORY	31,300
073	MEMORY EXPANSION UNIT	7,500
074	EXTENDED MEMORY KIT	2,000
(4) 046	BUFFERED BLOCK CHANNELS	10,800
072	I/O EXPANSION UNIT	8,500
022	REAL TIME CLOCK	1,750
052	PRIORITY INTERRUPT	3,150
6890A	75 IPS TAPE DRIVE WITH CONTROLLER	24,600
1150	VULCAN OPERATING SYSTEM SOURCE	3,000
1310	SORT/MERGE	300
1411	FORTRAN 77	7,500
1415	FORTRAN LOAD AND GO	500
1431	EXTENDED BASIC	5,000
1720	TX TEXT EDITOR	250
1710	FORMAT LISTING UTILITY	250
1530	AZ7 QUERY LANGUAGE AND REPORT WRITER	9,500
		\$281,800
CHOOSE ONE:		
(4) 5530-C	69 MB DISKS AND CONTROLLERS	107,600
(4) 5550-C	263 MB DISKS AND CONTROLLERS	174,600
(1) & (2) 5550-C	263 MB DISK AND CONTROLLER	186,170
5660	592 MB DISKS AND CONTROLLERS (5660 NON-REMOVABLE)	
	PRICE OF HARRIS SYSTEM 800 VERSION A (276 MB)	\$389,400
	PRICE OF HARRIS SYSTEM 800 VERSION B (1052 MB)	\$456,400
	PRICE OF HARRIS SYSTEM 800 VERSION C (1447 MB)	\$467,970

TABLE E-49
HIGH CAPACITY CONFIGURATION AND PRICE
MODCOMP CLASSIC 7870

MODEL #	DESCRIPTION	PRICE
7870-H67B	MODCOMP CLASSIC 7870 WITH 1 MB MEMORY, PACKAGE	\$133,500
4157-1	TAPE DRIVE AND CONTROLLER CREDIT	-21,200
5553	75 IPS TRI-DENSITY TAPE DRIVE AND CONTROLLER	<u>42,700</u>
		\$155,000
FOR VERSION B ONLY:		
3648	MEMORY EXPANSION ASSEMBLY	6,850
(2) 3692	512 KB MEMORY	56,000
4174-1-67A	67 MB DISK DRIVE AND CONTROLLER PACKAGE CREDIT	-27,800
4174-5-256A	256 MB DISK DRIVE AND CONTROLLER PACKAGE	<u>42,250</u>
		\$ 77,300
4903	PERIPHERAL CONTROLLER INTERFACE	2,200
4701-1	INTERVAL TIMER	1,100
(3) 3771	DUAL BUS I/O PROCESSORS	22,500
4911	PERIPHERAL CONTROLLER ENCLOSURE	2,675
0001	19 INCH CABINET	1,325
	FORTRAN 77	5,000
	PASCAL	5,000
	MAX IV OPERATING SYSTEM SOURCE	900
	INFINITY DATABASE MANAGER	<u>10,000</u>
		\$ 50,700
CHOOSE ONE:		
(3) 4174-1-67A	67 MB DISK DRIVES AND CONTROLLERS PACKAGES	111,200
(3) 4174-1-256A	256 MB DISK DRIVES AND CONTROLLERS PACKAGES	126,750
	PRICE OF MODCOMP 7870 VERSION A (1 MB, 268 MB DISK)	\$316,900
	PRICE OF MODCOMP 7870 VERSION B (2 MB, 1,024 MB DISK)	\$409,750

TABLE E-50
HIGH CAPACITY CONFIGURATION AND PRICE
PRIME 750 VERSIONS A AND B

MODEL #	DESCRIPTION	PRICE
CHOOSE ONE:		
750-1MB	PRIME 750 1 MB SYSTEM	\$154,000
750-2MB	PRIME 750 2 MB SYSTEM	\$180,000
7551	SERIES 50 EXPANSION CABINET	2,500
	125 IPS TAPE DRIVE AND INTERFACE	25,000
8532-P	PL/I LANGUAGE	12,000
8510-P	FORTRAN 77 LANGUAGE	4,500
8538-P	SOURCE LEVEL DEBUGGER	1,500
8562-P	PRIME/POWER QUERY DATA MANAGER	12,500
8520-M	BASIC LANGUAGE	<u>5,000</u>
		\$ 63,000
CHOOSE ONE:		
(4) 4361	80 MB DISKS AND CONTROLLERS (77 MB)	\$108,000
(4) 4371	300 MB DISKS AND CONTROLLERS (292 MB)	\$168,000
	PRICE OF PRIME 750 VERSION A	\$325,000
	PRICE OF PRIME 750 VERSION B	\$411,000

TABLE E-51
HIGH CAPACITY HOST CONFIGURATION AND PRICE
DATA GENERAL ECLIPSE MV/8000 VERSIONS A AND B

MODEL #	DESCRIPTION	PRICE
CHOOSE ONE:		
9350-C	ECLIPSE MV/8000 1,024 KB 4 WAY INTERLEAVED MEMORY, 6026 TAPE DRIVE, 6122 DISK (277 MB)	\$175,900
9360-C	ECLIPSE MV/8000 2,048 KB 4 WAY INTERLEAVED MEMORY, 6122 DISK (277 MB)	203,900
6108	DASHER D200 CONSOLE TERMINAL	1,950
4065	I/O INTERFACE FOR 4068	200
4191	I/O INTERFACE FOR 4068	400
4068	PROGRAMMABLE INTERVAL TIMER FLOATING POINT PROCESSOR	600 6,195
3822-24R	DTOS MICRONOVA DIAGNOSTICS ON FICHE	25
3826-24R	DTOS ECLIPSE MV/8000 DIAGNOSTICS ON FICHE	25
3900-00H	AOS/VS OPERATING SYSTEM	10,000
3900-30H	AOS/VS OPERATING SYSTEM SOURCE	15,000
3901-00H	AOS/VS FORTRAN 77	5,000
3901-35H	AOS/VS FORTRAN 77 RUN TIME SOURCE	3,000
3901-00H	INFOS II FILE MANAGEMENT	2,500
3913-01H	INFOS II QUERY	2,000
3915-01H	SORT/MERGE	750
3938-01H	SWAT DEBUGGER	2,000
3906-02H	DG/L SYSTEMS LANGUAGE	5,700
3905-00H	BASIC	4,000
		\$ 59,345
CHOOSE ONE PAIR:		
6060	96 MB DISK SUBSYSTEM AND CONTROLLER	25,800
(3) 6060-H	96 MB DISKS AND CONTROLLERS	83,400
6061	190 MB DISK SUBSYSTEM AND CONTROLLER	31,000
(3) 6122	277 MB DISK SUBSYSTEMS AND CONTROLLERS	115,500
	PRICE OF DG ECLIPSE MV/8000 VERSION A	\$344,445
	PRICE OF DG ECLIPSE MV/8000 VERSION B	\$409,745

TABLE E-52
 HIGH CAPACITY HOST AND ARRAY PROCESSOR
 CONFIGURATION AND PRICE
 SEL 32/7780 MODEL 2530 VERSION A

MODEL #	DESCRIPTION	PRICE
2530	32/7780 CONFIGURATION WITH 1 MB MEMORY; (2) IPUS, HSFPS, SAS	\$125,000
2537	PCS TO WCS (WRITEABLE CONTROL STORE UPGRADE)	4,000
2538	45 IPS TO 125 IPS AND TRIDENSITY TAPE UPGRADE	30,000
2348	EXPANSION LOGIC CHASSIS	5,830
2345	REAL TIME OPTION MODULE	3,180
8191	DISK PROCESSOR EIGHT DRIVE OPTION	1,000
9520	(3) 67 MB FORMATTED MASTER DISKS AND CONTROLLERS	72,825
1401-0123	MPX-32 SOURCE	6,000
1413-0103	FORTRAN 77	4,000
1414-0103	PASCAL	5,800
1410-0103	SCIENTIFIC ACCELERATOR PACKAGE	2,700
1410-0123	SCIENTIFIC ACCELERATOR PACKAGE SOURCE	5,500
1514-0103	SYMBOLIC DEBUGGER	1,500
1201-0103	STATISTICAL SUBROUTINE LIBRARY	1,000
1385-9123	USER'S GROUP LIBRARY I	175
1386-9123	USER'S GROUP LIBRARY II	<u>175</u>
		\$268,685
ARRAY PROCESSOR		
9274	VPU 3300 CM ARRAY PROCESSOR	48,500
2432	VP PROGRAMMER'S PANEL	2,100
2435	VP POWER SUPPLY	1,150
2427	VP TYPE III CHASSIS OPTION	3,650
9164	VP I/O SCROLL TYPE 4	4,200
(5) 2458	170 NS 64 KB VP MEMORY MODULES	<u>107,500</u>
		\$167,100
	PRICE OF SEL 32/7780 (2530) VERSION A WITH AP	\$435,785

TABLE E-53

HIGH CAPACITY HOST AND ARRAY PROCESSOR

CONFIGURATION AND PRICE

SEL 32/7780 MODEL 2531 VERSIONS B & C

MODEL #	DESCRIPTION	PRICE
2531	32/7780 CONFIGURATION WITH 2 MB MEMORY; (2) IPUS, HSFPS, SAS	\$145,000
2537	PGS TO WCS (WRITEABLE CONTROL STORE UPGRADE)	4,000
2538	45 IPS to 125 IPS AND TRIDENSITY TAPE UPGRADE	30,000
2348	EXPANSION LOGIC CHASSIS	5,830
2345	REAL TIME OPTION MODULE	3,180
8191	DISK PROCESSOR EIGHT DRIVE OPTION	1,000
9523	(3) 256 MB FORMATTED MASTER DISKS AND CONTROLLERS	128,790
1401-0123	MPX-32 SOURCE	6,000
1413-0103	FORTRAN 77	4,000
1414-0103	PASCAL	5,800
1410-0103	SCIENTIFIC ACCELERATOR PACKAGE	2,700
1410-0123	SCIENTIFIC ACCELERATOR PACKAGE SOURCE	5,500
1514-0103	SYMBOLIC DEBUGGER	1,500
1201-0103	STATISTICAL SUBROUTINE LIBRARY	1,000
1385-9123	USER'S GROUP LIBRARY I	175
1386-9123	USER'S GROUP LIBRARY II	<u>175</u> \$344,650
ARRAY PROCESSOR		
9274	VPU 3300 CM ARRAY PROCESSOR	48,500
2432	VP PROGRAMMER'S PANEL	2,100
2435	VP POWER SUPPLY	1,150
2427	VP TYPE III CHASSIS OPTION	3,650
9164	VP I/O SCROLL TYPE 4	4,200
(5) 2458	170 NS 64 KB VP MEMORY MODULES	<u>107,500</u> \$167,100
(4) 2458	170 NS 64 KB VP MEMORY MODULES FOR VERSION C ONLY	\$ 86,000
	PRICE OF SEL 32/7780 (2531) VERSION B WITH AP	\$511,750
	PRICE OF SEL 32/7780 (2531) VERSION C WITH AP	\$597,750

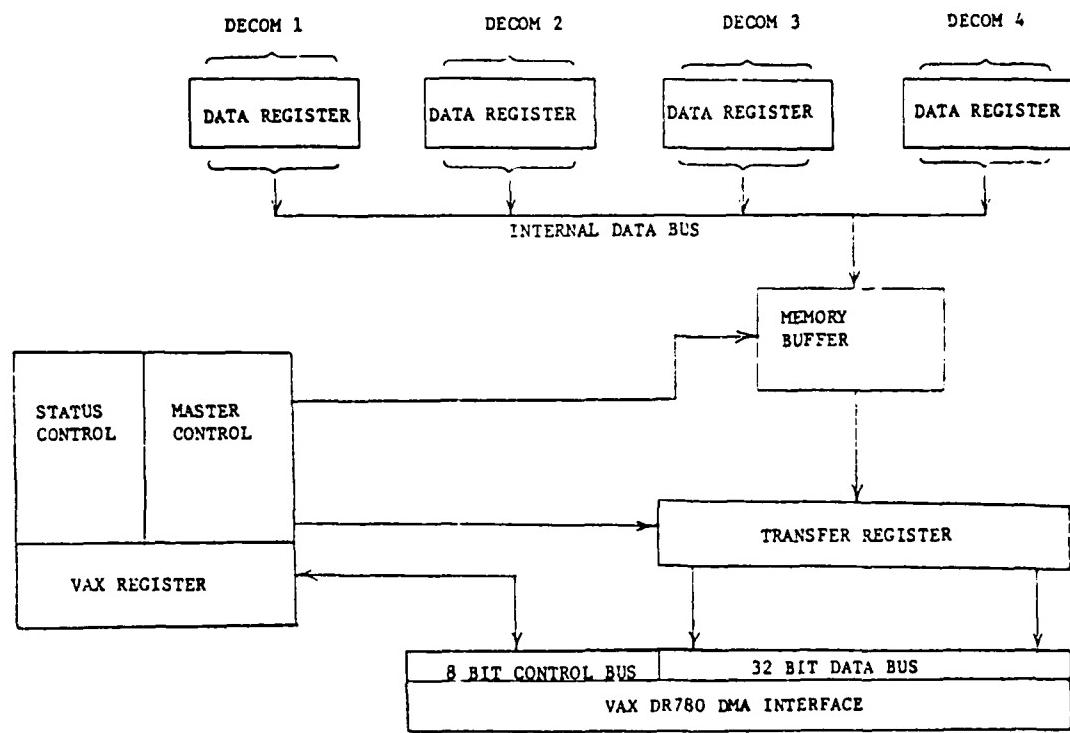


FIGURE E-21
OVERVIEW OF THE VAX 11/780 QUAD DECOM INTERFACE

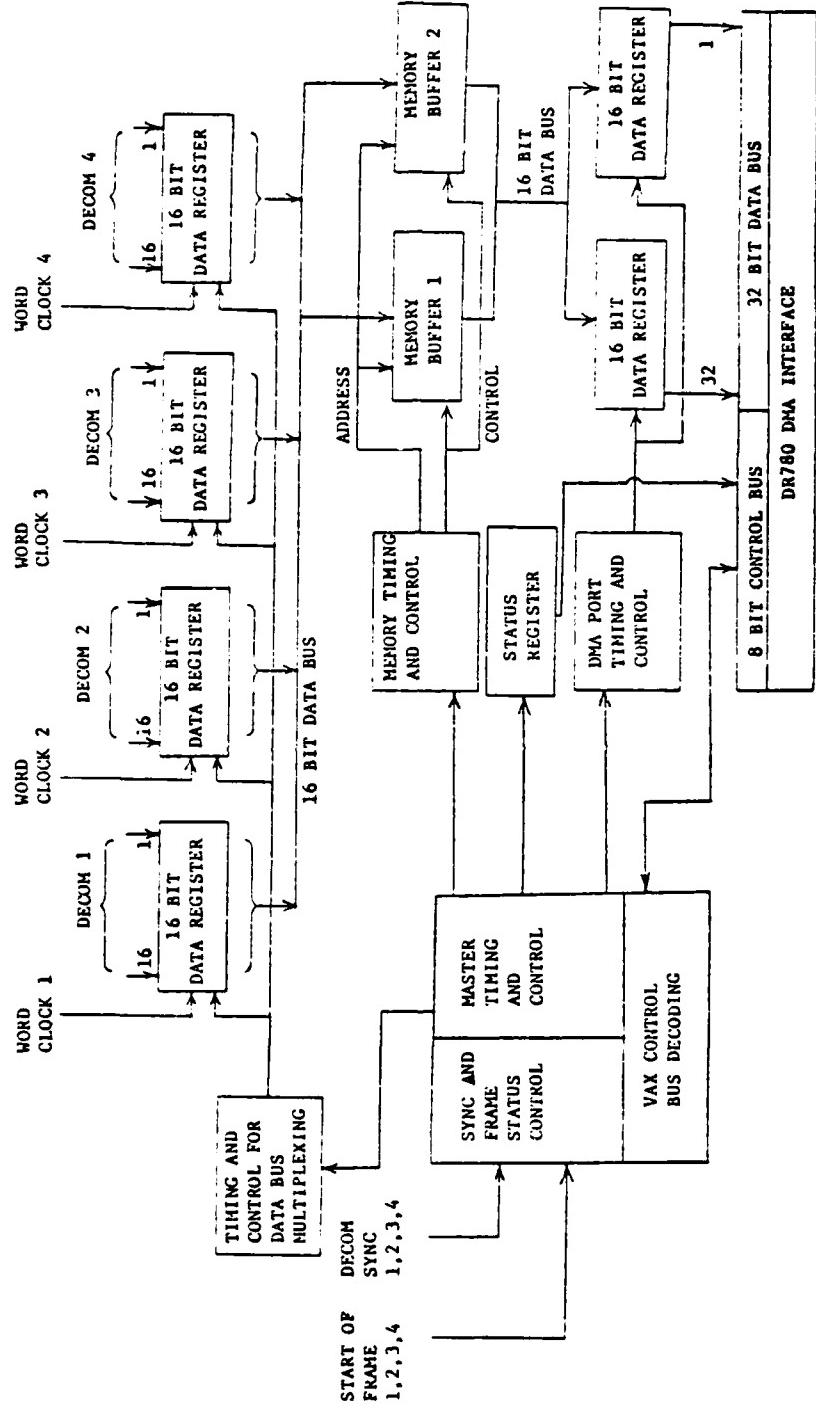


FIGURE E-22
VAX 11/780 QUAD DECOM INTERFACE

ADDENDUM
EVALUATION OF RETICON R5609
SWITCHED-CAPACITOR LOW-PASS FILTER

(A REPORT OF TESTS CONDUCTED AT MCAIR 16 - 24 JULY 1980)

ABSTRACT: Three Reticon R5609 Switched-Capacitor low-pass filters in plastic packages were purchased and temperature tested over the range -55°C to 100°C. Temperature performance varied considerably as a function of the input clock frequency used to determine the filter cutoff. DC offset drift was very poor with a low clock frequency, and filter characteristics were poor with a high clock frequency. Good performance was exhibited with a clock frequency of 500 KHz (cutoff frequency 5 KHz). All three filters failed during the course of testing.

1. INTRODUCTION

The R5609 is an "all-silicon" variable bandwidth analog low-pass filter packaged in an 8-pin "mini-DIP". It uses switched-capacitor techniques - therefore, no external components are required to achieve the filter characteristics; however, a clock input is required to set the filter to the desired bandwidth (clock rate is 100 times the 3 dB bandwidth). The filter is a seventh order elliptic with nominal .2 dB passband ripple and 75 dB stopband minima. The bandwidth can be varied from .1 Hz to 25 KHz by adjusting the clock input frequency.

Analog sampling (at a rate equal to one-half the clock frequency) is employed internally in the filter, hence, it is subject to aliasing. A supplemental anti-alias filter may, therefore, be required to remove frequencies above 0.49 times the clock frequency from the input to the R5609. Reticon suggests using a one or two pole filter for this purpose; however, three poles are required in order to ensure adequate anti-aliasing protection and minimal degradation of the desired passband. A three-pole Butterworth with 3 dB cutoff set at 0.02 times the R5609 clock frequency will suffice.

Other external circuitry may be required for offset nulling, clock residue filtering, and device protection from inputs with power off.

Temperature specifications for Reticon switched-capacitor filters are as yet unavailable. Since the R5609 is a potential candidate for high performance anti-alias filtering in an airborne PCM data system, an evaluation including temperature testing was performed.

For applications involving temperature extremes, the factory recommends units in ceramic packages; however, no such units were available in June 1980. Therefore, our evaluation was performed on the standard plastic packaged units that were available.

2. SUMMARY OF RESULTS

Three R5609 low-pass filters were purchased and tested. All three units were operational at the start of the tests. One unit became inoperative at room temperature before data was taken. The remaining two units also eventually failed (after extensive operation and temperature testing) during power-down at 100°C. The failure mode exhibited by all three filters is the output remains at approximately the negative supply voltage.

The filters were tested at three clock frequencies: 2 MHz, 500 KHz, and 2KHz, corresponding to nominal 3 dB bandwidths of 20 KHz, 5 KHz, and 20 Hz, respectively. The test data are summarized in Tables E-54, E-55, and E-56. All of the data summarized was taken from the same filter. Marked differences in temperature performance were noted at the different clock frequencies. The best overall performance occurred with the 500 KHz clock (5 KHz bandwidth). Filter characteristics were remarkably stable (only 2° phase shift variation at cutoff and no discernible variations in passband ripple or insertion gain, from -55°C to 80°C). DC stability was reasonably good (1.6% F.S. offset shift from 25°C to 80°C). Note F.S. = 12 volts peak to peak.

With the KHz clock (20 Hz bandwidth), the DC stability was very poor at high temperatures (10% F.S. offset at 80°C and 30% F.S. offset at 100°C). The filter characteristics remained good, with only 4° phase variation from -55°C to 80°C.

With the 2 MHz clock (20 KHz bandwidth), the DC stability was good (1.5% F.S. offset variation); however, the filter characteristics varied considerably with temperature. The phase shift at cutoff varied 36° and considerable peaking (1.8 dB) occurred in the passband.

Measured transition ratio (ratio of passband edge frequency to stopband edge frequency) and filter performance (passband ripple and stopband rejection)

in most cases exceeded the theoretical performance of a sixth-order elliptic, thus, verifying that the filter is indeed a seventh-order elliptic. The stop-band rejection was 7-19 dB less than the specified 75 dB ; however, this is probably because the input signal level used was 12 dB below full-scale (only 500 MV RMS was available from the random noise generator in the HP3582A Spectrum Analyzer). The measured clock residue noise was considerably higher than the typical 25 MV RMS indicated on the data sheet. The DC offset and clock residue appear to be functions of both the clock frequency and amplitude.

3. RECOMMENDATIONS

Test results with the 500 KHz clock were encouraging. However, the poor performance at the other clock rates coupled with the devices requirement for a supplemental anti-alias filter may restrict the usefulness of the device as a general purpose or variable filter. Prior to passing final judgement on the R5609's suitability for use in an airborne PCM system, testing of units in ceramic packages is recommended. Further testing should include many clock frequencies to better define the operating limits of the device.

A more detailed data sheet (including temperature limits) and an application note regarding handling precautions should be solicited from Reticon.

4. TEST DESCRIPTION

A diagram of the test setup is shown in Figure E-23. All of the measurements indicated in Tables E-54, E-55 and E-56, except for clock residue and DC offset were obtained using the HP3582A Spectrum Analyzer. This is a two-channel fast Fourier instrument featuring a built-in band-limited random noise source. The noise source was used as the filter input and, also, as the reference for the transfer function measurements. The filter output was routed to the other input of the analyzer. The RMS averaging mode was used, with 256 averages taken to ensure a high degree of statistical accuracy for the measurements. The analysis range, frequency resolution, and measurement times are indicated below for the three filter clock frequency test setups:

R5609 FILTER			HP3582A	
<u>CLOCK FREQ.</u>	<u>CUTOFF FREQ.</u>	<u>ANALYSIS RANGE</u>	<u>f</u>	<u>TOTAL TIME</u>
2 KHz	20 Hz	50 Hz	.4 Hz	640 SEC.
500 KHz	5 KHz	10 KHz	80 Hz	3.2 SEC.
2 MHz	20 KHz	25 KHz	200 Hz	1.28 SEC.

The maximum range of the HP3582A (25 KHz) was not sufficient to examine the stopband characteristics of the 20 KHz filter; hence the omissions in Table E-56.

Transfer function magnitude and phase and coherence spectrum measurements for all three clock frequencies at room temperature are shown in Figures E-24 through E-30. These are photos taken of the HP3582A display screen. The "marker" on the HP3582A was used for determining the transition ratio, passband ripple, stopband rejection, and phase measurements at individual frequencies.

DC offset measurements were made using a digital voltmeter with the R5609

filter input shorted. Clock residue measurements were made with an oscilloscope.

Figures E-31 through E-33 show results at room temperature.

Output noise RMS was calculated by integrating spectral measurements made on the HP3582A (see Figure E-34) from 0 to 1/2 the sample rate, ignoring anomalies such as 60 Hz and its harmonics and the alias of the sampling frequency appearing at DC.

TABLE E-54
TEST DATA

SWITCHED CAPACITOR FILTER (RETICON R5609 LOW-PASS)
CLOCK FREQUENCY 2 kHz NOMINAL CUTOFF 20 Hz

	<u>-55°C</u>	<u>-20°C</u>	<u>25°C</u>	<u>70°C</u>	<u>80°C</u>	<u>100°C</u>	<u>SPEC.</u>
TRANSITION RATIO	.561	.584	.519	.529	.538	-	-
STOPBAND REJECTION	65.4 dB	55.6 dB	66.5 dB	68.7 dB	60.0 dB	-	75dB
-3dB FREQUENCY	19.6 Hz	19.6 Hz	19.6 Hz	19.6 Hz	19.6 Hz	-	19.4 - 20.6 Hz
PHASE @ -3dB	-403°	-402°	-401°	-405°	-404°	-	-
PASSBAND EDGE	18.4 Hz	18.0 Hz	16.8 Hz	18.0 Hz	16.8 Hz	-	-
PHASE @ PASSBAND EDGE	-344°	-329°	-293°	-332°	-293°	-	-
PASSBAND RIPPLE	.3dB	.1dB	.4dB	.3dB	.2dB	-	.2dB
INSERTION GAIN	-.15dB	-.15dB	-.20dB	-.25dB	-.20dB	-	+.4dB
DC OFFSET	-	-	0	-	-1142mV	-3620mV	-
OUTPUT NOISE	1.8mV RMS	1.8mV RMS	.42mV RMS	-	4mV RMS	-	2.5mV RMS
CLOCK RESIDUE	-	-	165mV(P-P)	-	220mV(P-P)	300mV(P-P)	25mV RMS
FILTER ORDER	>6	>6	>5	>6	>5	-	7

TABLE E-55
TEST DATA

SWITCHED CAPACITOR FILTER (RETICON R5609 LOW-PASS)
CLOCK FREQUENCY 500 KHz NOMINAL CUTOFF 5 KHz

	<u>-55°C</u>	<u>-20°C</u>	<u>25°C</u>	<u>70°C</u>	<u>80°C</u>	<u>100°C</u>	<u>SPEC.</u>
TRANSITION RATIO	.529	.541	.569	.544	.566	-	-
STOPBAND REJECTION	65.6dB	67.4dB	65.6dB	66.1dB	58dB	-	75dB
-3dB FREQUENCY	4960 Hz	4960 Hz	4960 Hz	4960 Hz	4960 Hz	-	4850 - 5150 Hz
PHASE @ -3dB	-415°	-414°	-414°	-416°	-415°	-	-
PASSBAND EDGE	4400 Hz	4430 Hz	4640 Hz	4480 Hz	4480 Hz	-	-
PHASE @ PASSBAND EDGE	-316°	-327°	-350°	-328°	-328°	-	-
PASSBAND RIPPLE	.2dB	.2dB	.2dB	.2dB	.2dB	-	.2dB
INSERTION GAIN	-1dB	-1dB	-1dB	-1dB	-1dB	-	+-.4 dB
DC OFFSET	-	-	-	72mV	-	-119mV	-
OUTPUT NOISE	-	-	-	-	-	-	2.5mV RMS
CLOCK RESIDUE	-	-	.650mV(P-P)	-	2.65VP-P	-	25mV RMS
FILTER ORDER	>6	>6	>6	>6	>5	-	7

TABLE E-56
TEST DATA

SWITCHED CAPACITOR FILTER (RETICON R5609 LOW-PASS)
CLOCK FREQUENCY 2MHz
NOMINAL CUTOFF 20 kHz

	<u>-55°C</u>	<u>-20°C</u>	<u>25°C</u>	<u>70°C</u>	<u>80°C</u>	<u>100°C</u>	<u>SPEC.</u>
TRANSITION RATIO	-	-	-	-	-	-	-
STOPBAND REJECTION	-	-	-	-	-	-	75dB
-3dB FREQUENCY	19800 Hz	19800 Hz	19800 Hz	19800 Hz	19800 Hz	-	19400 - 20600 Hz
PHASE @ -3dB	-423°	-424°	-435°	-455°	-456°	-	-
PASSBAND EDGE	18800 Hz	18800 Hz	19200 Hz	19200 Hz	19200 Hz	-	-
PHASE @ PASSBAND EDGE	-371°	-372°	-402°	-419°	-421°	-	-
PASSBAND RIPPLE	.2dB	.3dB	.7dB	1.6dB	1.8dB	-	.2dB
INSERTION GAIN	0dB	+.05dB	+.35dB	+.8dB	+0.9dB	-	±.4dB
DC OFFSET	-	-	75mV	-	-107mV	-	-
OUTPUT NOISE	-	-	-	-	-	-	2.5mV RMS
CLOCK RESIDUE	-	-	2.4V(P-P)	-	2.4V(P-P)	-	2.5mV RMS
FILTER ORDER	-	-	-	-	-	-	7

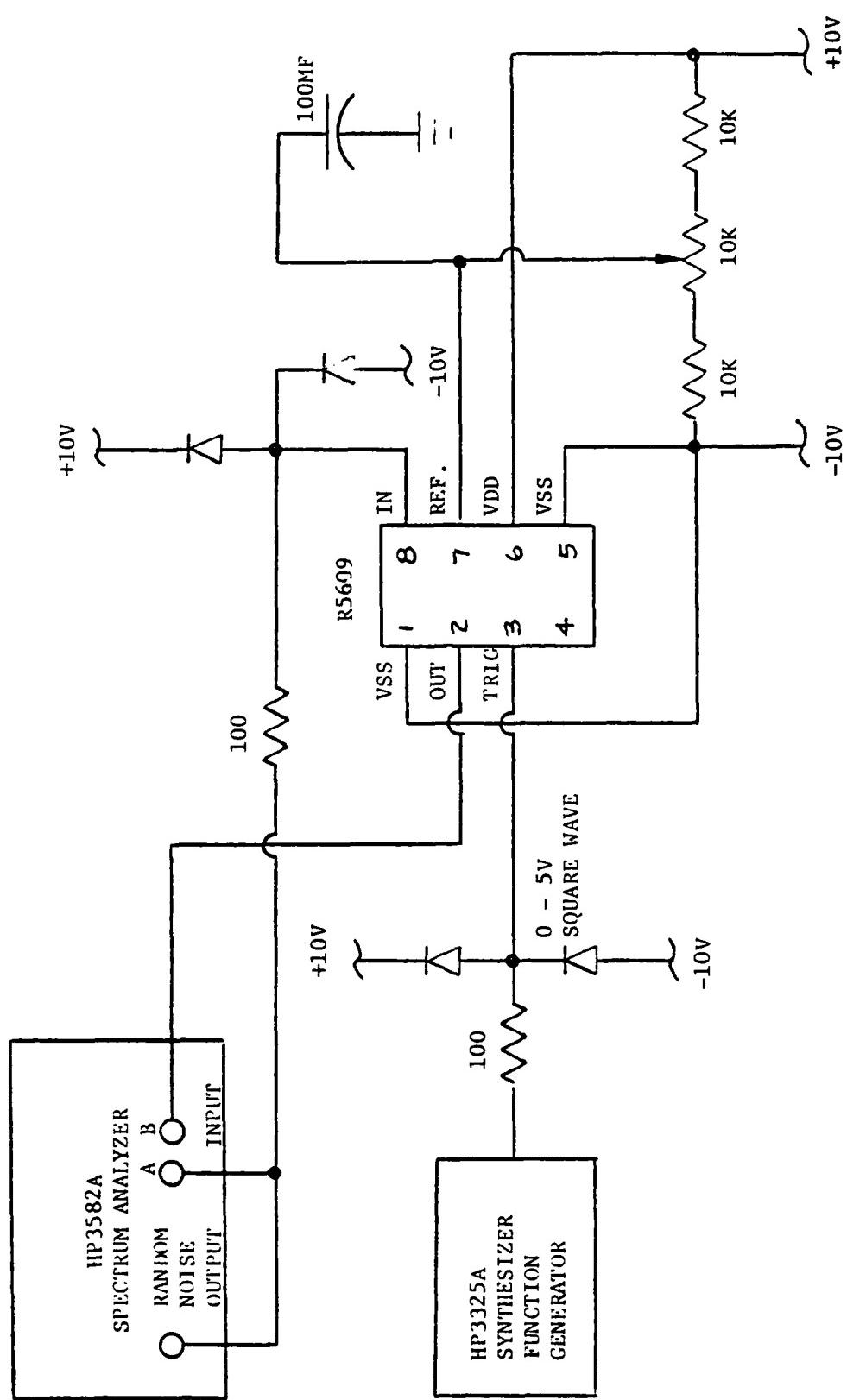


FIGURE E-23
TEST SETUP FOR RETICON R5609 FILTER EVALUATION

FIGURE E-24
R5609 TRANSFER FUNCTION
MAGNITUDE, 2 KHz CLOCK,
25°C

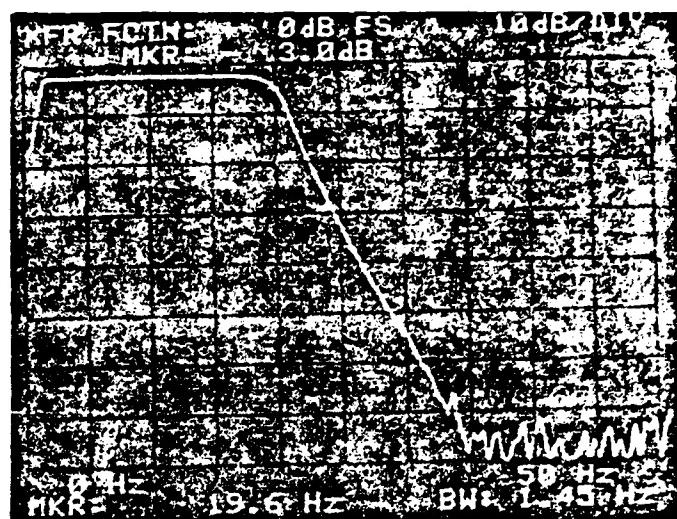


FIGURE E-25
R5609 TRANSFER FUNCTION
PHASE, 2 KHz CLOCK, 25°C

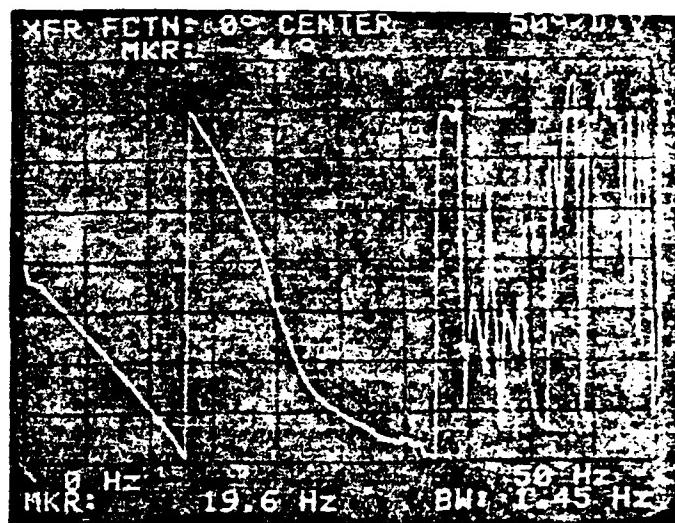


FIGURE E-26
R5609 COHERENCE SPECTRUM
2 KHz CLOCK, 25°C

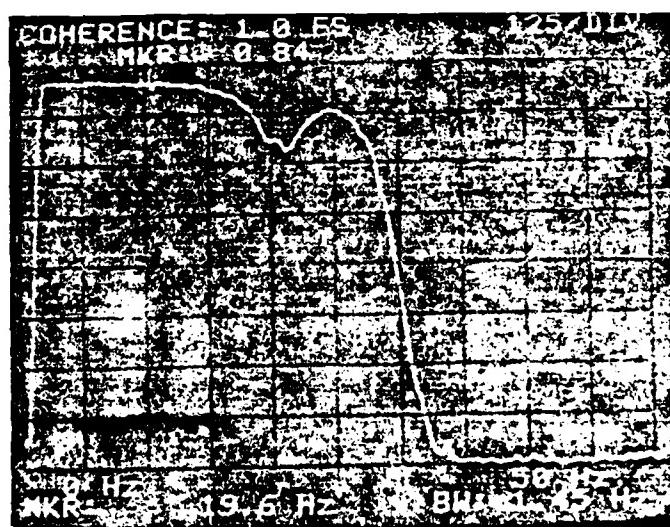




FIGURE E-27
R5609 TRANSFER FUNCTION MAGNITUDE AND PHASE, 500 KHz CLOCK, 25°C

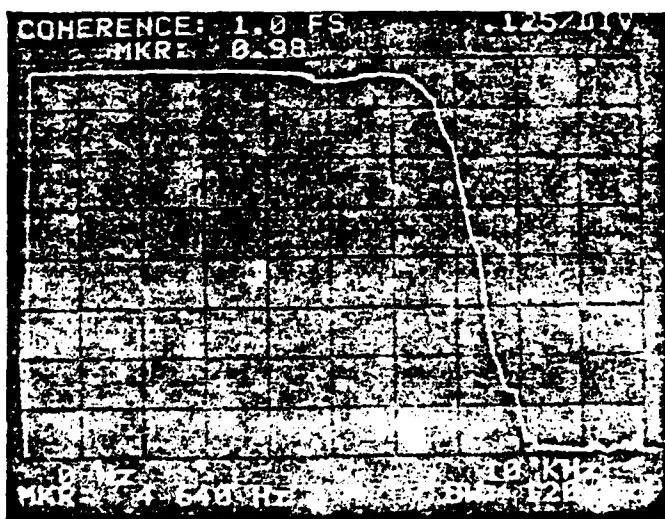


FIGURE E-28
R5609 COHERENCE SPECTRUM, 500 KHz CLOCK, 25°C

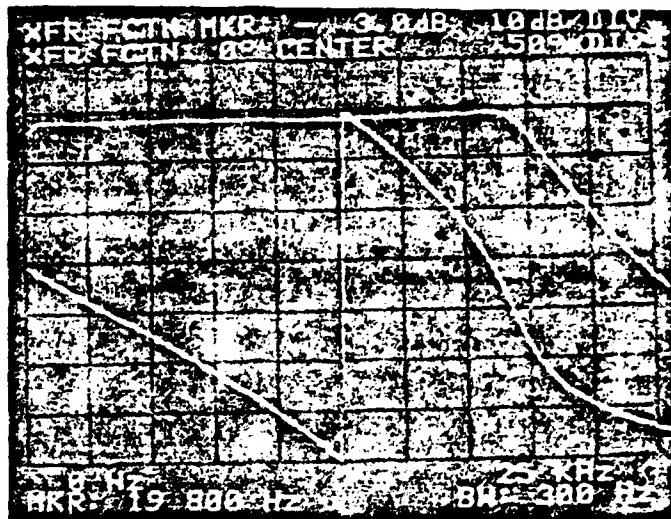


FIGURE E-29
R5609 TRANSFER FUNCTION MAGNITUDE AND PHASE, 2 MHz CLOCK, 25°C

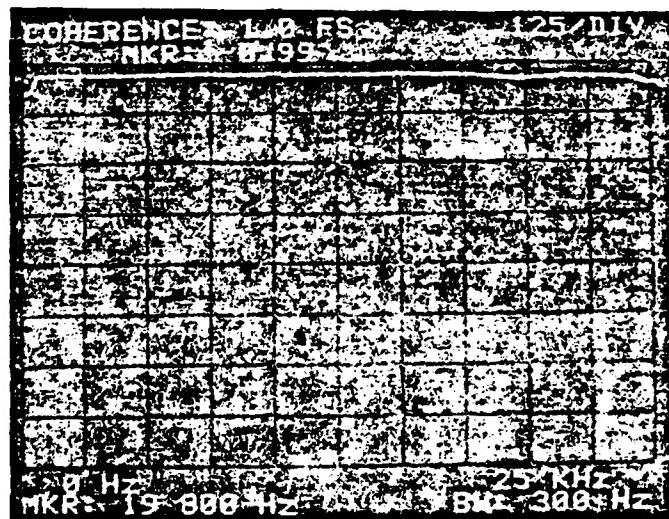


FIGURE E-30
R5609 COHERENCE SPECTRUM, 2 MHz CLOCK, 25°C

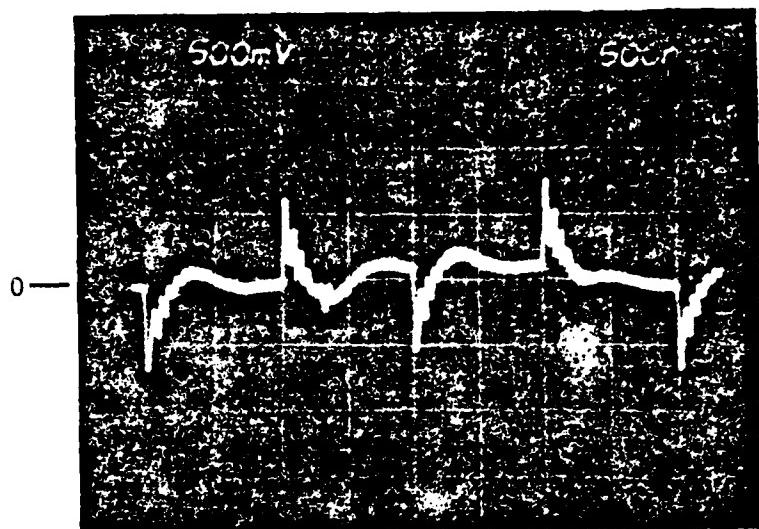


FIGURE E-31
R5609 CLOCK RESIDUE IN OUTPUT WITH INPUT SHORTED, 500 KHz CLOCK, 25°C, 500 MV/DIV, 500 NSEC/DIV

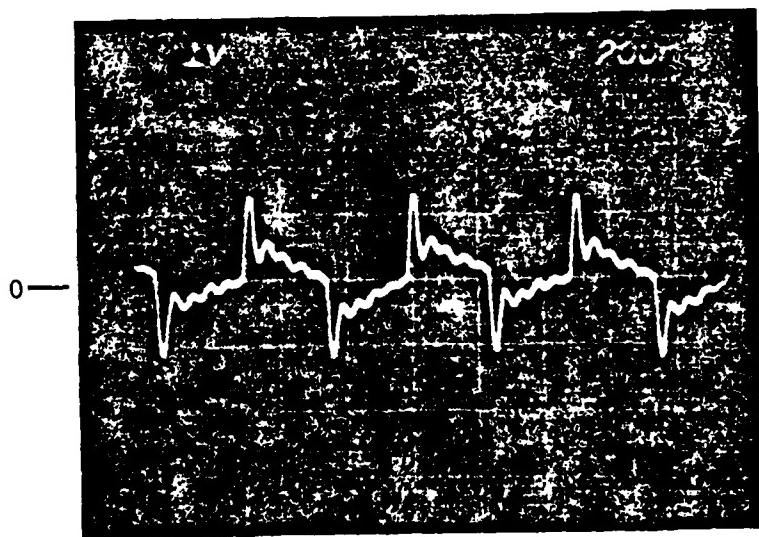


FIGURE E-32
R5609 CLOCK RESIDUE IN OUTPUT WITH INPUT SHORTED, 2 MHz CLOCK, 25°C, 1 V/DIV, 200 NSEC/DIV

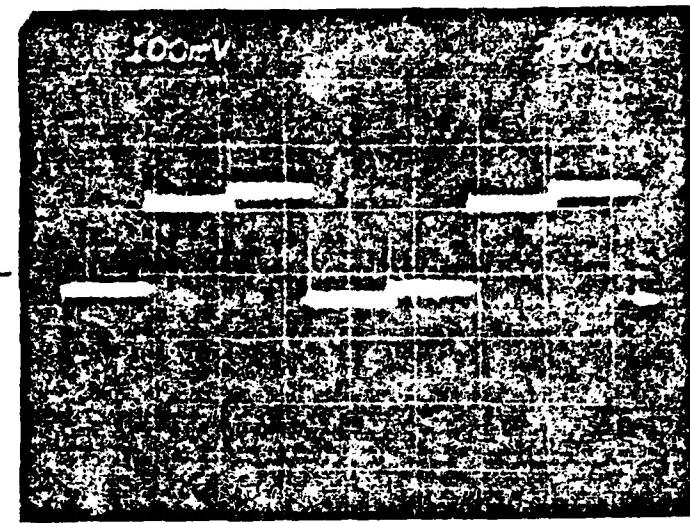


FIGURE E-33
R5609 CLOCK RESIDUE IN OUTPUT WITH INPUT SHORTED, 2 KHz CLOCK, 25°C,
100 MV/DIV, 200 SEC/DIV

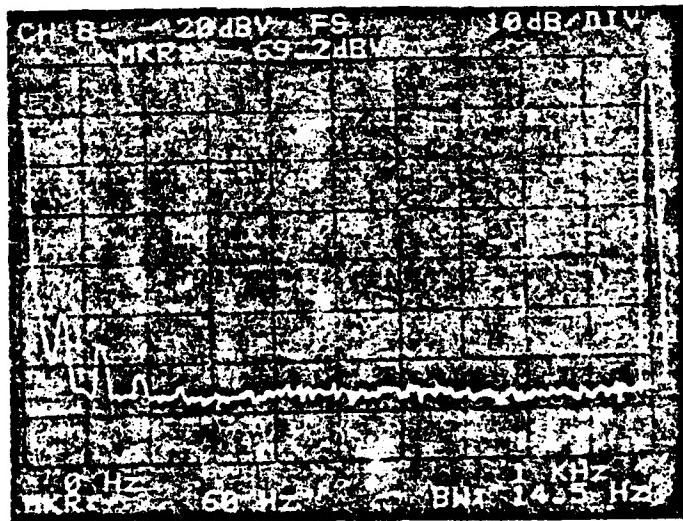


FIGURE E-34
R5609 SPECTRUM OF OUTPUT NOISE WITH INPUT SHORTED, 2 KHz CLOCK, 25°C